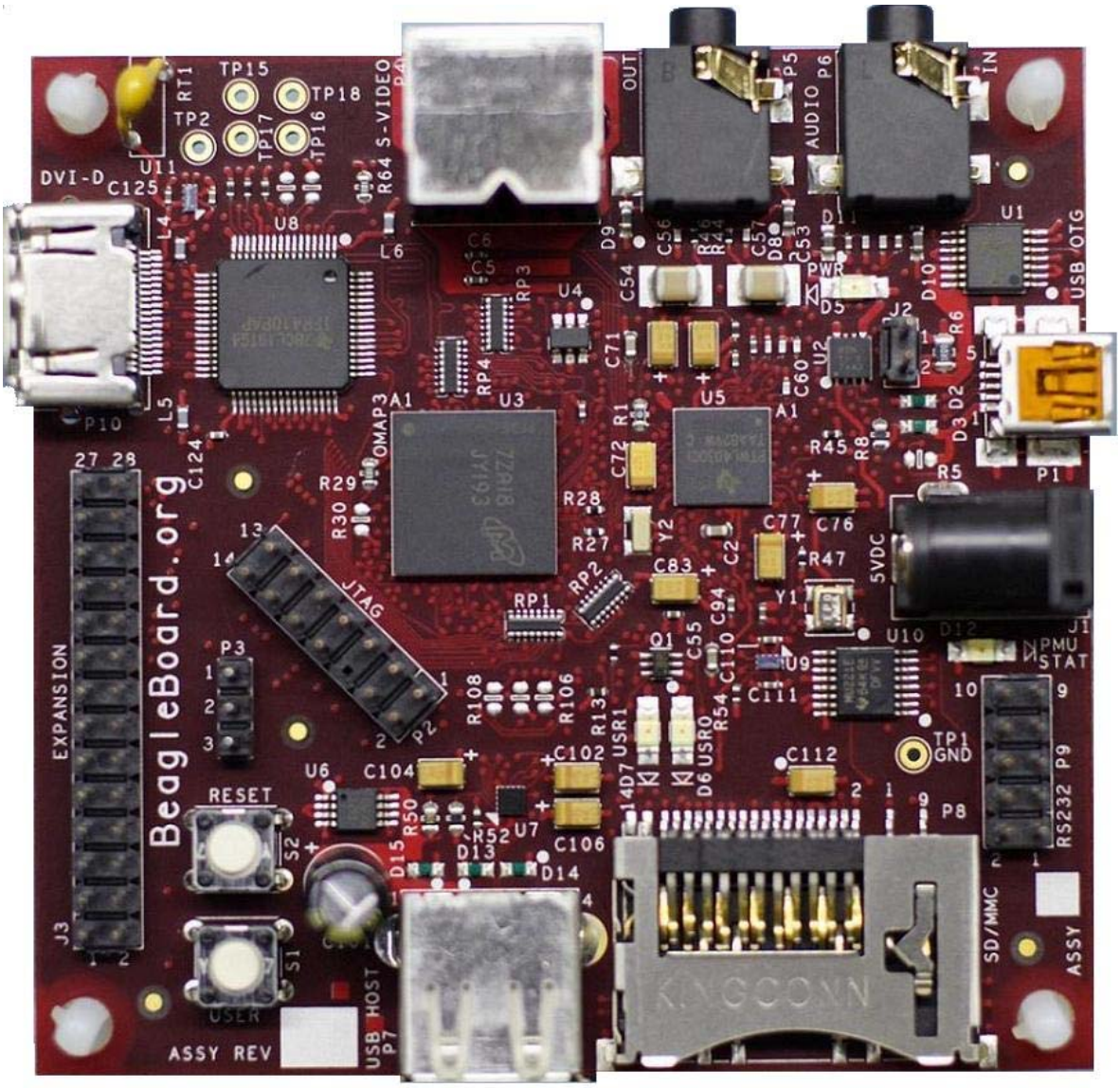

Beagle Rev A5
Hardware Reference Manual

Revision 0.5
April 4, 2008

For any questions, concerns, or issues submit them to gerald@beagleboard.org

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Table of Contents

Figures

Tables

1.0 Introduction

This document is the Hardware Reference Manual for the Beagle, a low cost OMAP3 based board supported through BeagleBoard.org. This document provides detailed information on the overall design and usage of the Beagle from a hardware perspective.

The key sections in this document are:

Section 2.0– Change History
This section provides tracking for the changes made to the Hardware Reference Manual.

Section 3.0– Definitions and references
This section provides definitions for commonly used terms and acronyms.

Section 4.0– Overview
This is a high level overview of the Beagle.

Section 5.0– Specification
Provided here are the features and electrical specifications of the Beagle.

Section 6.0Product Contents
This section describes what the beagle package looks like and what is included.

Section 7.0– Hookup
Covered here is how to connect the various cables to the Beagle.

Section 8.0– System Architecture and Design
This section provides information on the overall architecture and design of the Beagle. This is a very detailed section that goes deep into the design of each circuit.

Section 9.0– Connector Pinouts and Cables
The section describes each connector and cable used in the system. This will allow the user to create cables or to perform debugging as needed.

Section 10.0– Beagle Accessories
Covered in this section are a few of the accessories that may be used with Beagle. This is not an exhaustive list, but does provide an idea of the types of cables and accessories and how to find them. It also provides a definition of what they need to be.

Section 11.0 – Mechanical
Information is provided here on the dimensions of the Beagle.

Section 12.0 – Troubleshooting
Here is where you can find tips on trouble shooting the setup of the Beagle.

Section 13.0- Beagle Components
These are the top and bottom side silkscreen of the Beagle showing the location of the components.

Section 14.0- Beagle Schematics
These are the schematics for the Beagle itself.

Section 15.0- Beagle PCB Information
These are the schematics for the Beagle itself.

2.0 Change History

The **Table 1** tracks the changes made for each revision of this document.

Table 1. Change History

Rev	Changes	Date	By
0.1	1. Limited release for internal review.	1/09/08	GC
0.2	1. Limited interim release	1/30/08	GC
0.3	1. First broad release of the document.2	2/25/08	GC
0.4	1. Updated with Rev A3 data	3/5/08	GC

3.0 Definitions and References

3.1 Definitions

SD- Secure Digital
SDIO- Secure Digital Input Output
MMC- Multimedia Card
MDDR- Mobile Dual Data Rate
SDRAM- Synchronous Dual Access Memory
OMAP3- The CortexA8 based System on a Chip from Texas Instruments.

4.0 Beagle Overview

This board is an OMAP3 hardware platform to address the Open Source Community. It has been equipped with a minimum set of features to allow the user to experience the power of the OMAP3. It is not intended as a full development platform as many of the HW features and interfaces supplied by the OMAP3 are not accessible from Beagle. By utilizing standard interfaces, the Beagle is highly extensible to add many features and interfaces.

4.1 Beagle Usage Scenarios

The **Figure 1** provides an example of a few of the various usage scenarios for the Beagle.

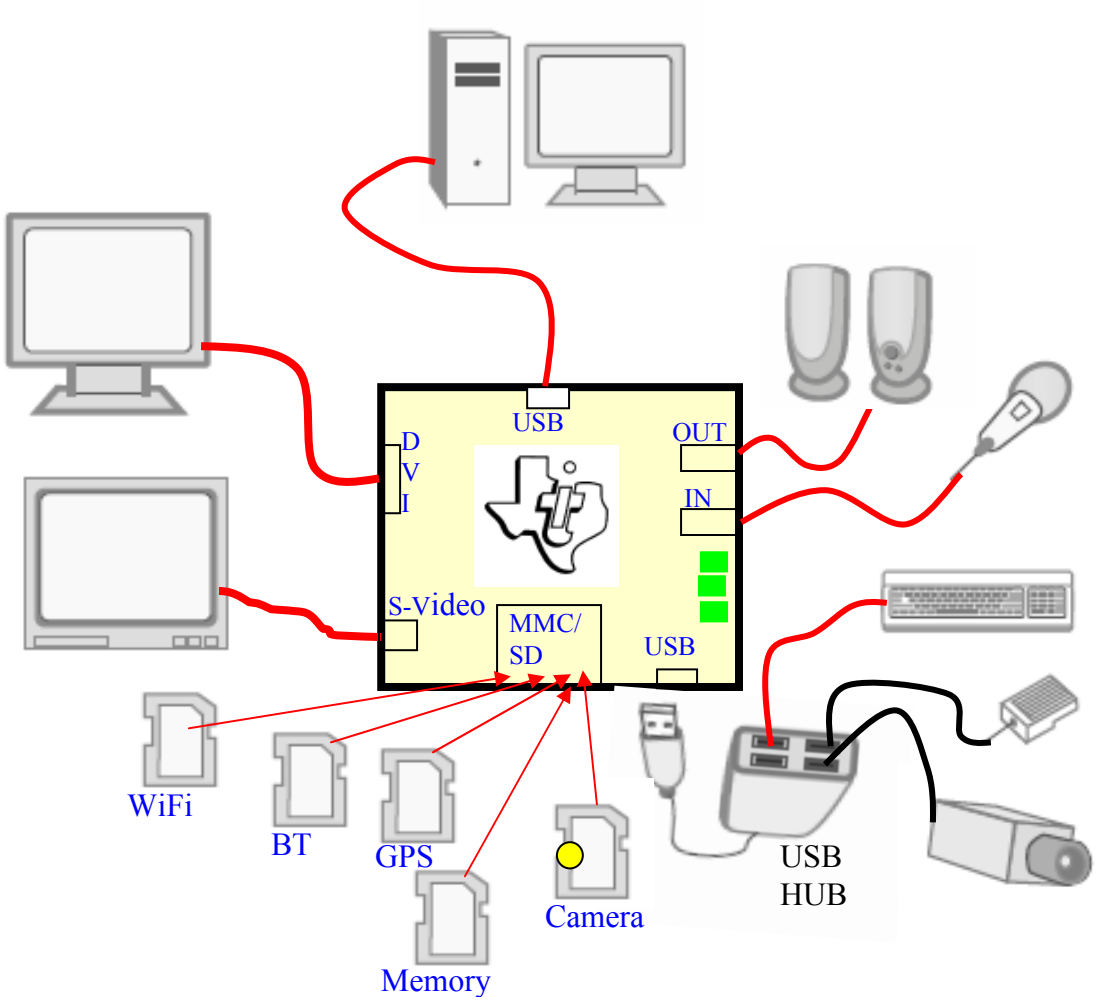

Figure 1. Beagle Usage Scenarios

5.0 Beagle Specification

This section covers the specifications of the Beagle. It also provides a high level description of the major components and interfaces that make up the Beagle.

5.1 Beagle Features

Table 2 provides a list of the Beagle's features.

Table 2. Beagle Features

	Feature	
Processor	OMAP3530 ES2.1	
POP Memory	Micron	
	2Gb NAND (256MB)	1Gb MDDR SDRAM (128MB)
TWL4030 PMIC	Power Regulators	
	Audio CODEC	
	Reset	
	USB Client PHY	
Debug Support	14-pin JTAG	GPIO Pins
	UART	LEDs
PCB	3.1" x 3.0" (78.74 x 76.2mm)	6 layers
Indicators	Power	2-User
	1-TWL4030 PWM	
HS USB 2.0 OTG Port	Mini AB USB connector	
	TWL4030 I/F	
	MiniAB	
HS USB 2.0 Host Port	Powered (5V)	
	Type A Connector	
	HS (480Mbps)	
Audio Connectors	3.5mm	
	L + R out	L+R Stereo In
SD/MMC Connector	6 in 1 SD/MMC/SDIO	4/8 bit support, Dual voltage
User Interface	1-User defined button	Reset Button
Video	DVI-D	S-Video
Power Connector	USB Power	DC Power
Expansion Connector	Power (5V & 1.8V)	UART
	McBSP	McSPI
	I2C	GPIO
	MMC	

The following sections provide more detail on each feature and components on the Beagle.

5.2 OMAP Processor

The Beagle uses the OMAP3 version ES2.1. It is in a .4mm pitch POP package. POP (Package on Package) is a technique where the memory, NAND and SDRAM, are mounted on top of the OMAP3. For this reason, when looking at the Beagle, you will not find an actual part labeled OMAP3.

5.3 Memory

The Micron POP memory is used on Beagle. It is mounted on top of the processor as mentioned. The key function of the POP memory is to provide:

- 2Gb NAND x 16 (256MB)
- 1Gb MDDR SDRAM x32 (128MB @ 166MHz)

No other memory devices are on the Beagle. It is possible however, that additional memory can be added to Beagle by installing a NAND based device in the SD/MMC slot.

5.4 TWL4030 Based Power Management

The TWL4030 is used to provide power to the Beagle with the exception of the 3.3V regulator which is used to provide power to the DVI-D encoder and RS232 driver. In addition to the power it also provides:

- Stereo Audio Out
- Stereo Audio in
- Power on reset
- USB Client PHY
- Status LED

5.5 HS USB 2.0 OTG Port

The HS USB OTG port is the primary power source and communication link for the Beagle and derives power from the PC over the USB cable. The client port is limited to 500mA by the PC. A single PC USB port is sufficient to power the beagle.

It is possible to take this to 1A by using a Y cable if additional power is needed or either the USB host port or an expansion card. **Figure 2** shows and example of the Y-Cable for the USB.

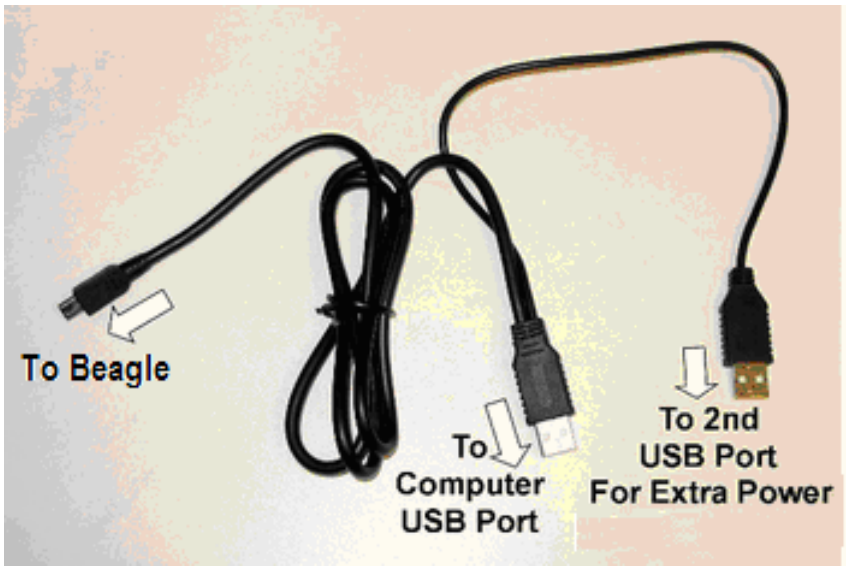

Figure 2. USB Y-Cable

The Beagle is supplied with a single minAB to USB A cable, so the user will need to supply the Y-Cable if needed. There is an option to provide external power to the Beagle using a 5V DC supply and is discussed later in this section.

5.6 HS USB 2.0 Host Port

A single Type A female connector is provided to access the onboard High Speed USB Host port. It will supply 5V power for such devices as keyboard, mice, and other powered devices. The amount of available current will depend on the amount of current remaining from the 500mA budget supplied by the standard USB port used to power the Beagle.

If an external 5V supply is used or if the Y-Cable is used, more current can be supplied via this port for powering higher current devices such as a USB HDD. On/Off control is provided on the 5V line and is under SW control via the OMAP3.

The HS USB Host port is limited to 480Mb/S. Low speed and full speed devices are not supported. If you need to connect LS or FS devices, an external hub is required.

5.7 Stereo Audio Output Connector

A 3.5mm standard stereo output audio jack is provided to access the stereo output of the onboard audio CODEC. The Audio CODEC is provided by the TWL4030.

5.8 Stereo Audio In connector

A 3.5mm standard stereo audio input jack is provided to access the stereo output of the onboard audio CODEC.

5.9 S-Video Connector

A 4 pin DIN connector is provided to access the S-Video output of the Beagle. This is a separate output from the OMAP processor and can contain different video output data from what is found on the DVI-D output.

It will support NTSC or PAL format output to a standard TV. The default is NTSC, but can be changed via the Software.

5.10 DVI-D Connector

The Beagle can drive a LCD panel equipped with a DVI-D digital input. This is the standard LCD panel interface of the OMAP3. It will support 24b color output. DDC2B (Display Data Channel) or EDID (Enhanced Display ID) support over I2C is provided in order to allow for the identification of the LCD monitor type.

The Beagle is equipped with a HDMI connector and it was selected for its small size. It does not support the HDMI interface and is used to provide the DVI-D interface only. The user must use a HDMI to DVI-D cable or adapter to connect to a LCD monitor. This cable or adapter is not provided with the Beagle.

5.11 SD/MMC 6 in 1 Connector

A 6 in 1 SD/MMC connector is provided as a means for expansion. It can support such devices as:

- WiFi Cards
- Camera
- Bluetooth Cards
- GPS Modules
- SD Memory Cards
- MMC Memory Cards
- SDIO Cards
- MMCMobile cards
- RS-MMC Cards
- miniSD Cards

It supports the MMC4.0 (MMC+) standard and can boot form the card. It will support both 4 and 8 bit cards. 8 Bit cards are at 1.8V only and the boot mode supports a 3V card.

One of the nicest features is that the OMAP3 can be booted from this connector. By holding the User button and forcing a reset, the Beagle will boot form this connector.

5.12 Reset Button

When pressed and released, causes a full power on reset of the Beagle.

5.13 User/Boot Button

A button is provided on the Beagle to provide multiple functions:

- When held while the reset button is pushed and released, will put the Beagle in a boot mode that will allow for the onboard Flash to be re-programmed by external software via the USB or Serial port.
- When held while reset button is pushed and released, will put the Beagle in a boot mode that will allow for the board to boot from the MMC slot as long as a card is plugged into the connector when the reset is done.
- Used as an application button that can be used by SW as needed.

5.14 Indicators

There are three green LEDs on the Beagle that can be controlled by the user.

- One on TWL4030 programmed via the I2C interface
- Two on the OMAP3 Processor controlled via GPIO pins

There is a fourth LED on the Beagle that provides an indication that power is supplied to the board and should always be on. This LED should be on in the USB powered mode and the DC supply mode.

5.15 Power Connector

Power will be supplied via the USB connector. If a need arises for additional power, such as when a board is added to the expansion connectors or there are higher loads on the USB Host supply, a larger wall supply 5V can be plugged into the optional power jack. When the wall supply is plugged in, it will remove the power path from the USB connector and will be the power source for the whole board. The power supply is not provided with the Beagle.

5.16 JTAG Connector

A 14 pin JTAG header is provided on the Beagle to facilitate the SW development and debugging of the board by using various JTAG emulators. The interface is at 1.8V.

5.17 RS232 Header

Support for RS232 via UART3 is provided. A 10 pin header is provided on the Beagle for access to an onboard RS232 transceiver is provided. It does require an IDC to DB9 flat cable, which is not provided, to access the serial port.

5.18 Expansion Headers

A single 24 pin header is provided on the board to allow for the connection of various expansion cards that could be developed by the users or other sources. Due to multiplexing, different signals can be provided on each pin providing more that 24 actual signal accesses.

5.19 Beagle Mechanical Specifications

Size: 3.0" x 3.1"
Max height: TBM
Layers: 6
PCB thickness: .062"
RoHS Compliant Yes
Weight: TBW

5.20 Electrical Specifications

Table 3 is the electrical specification of the external interfaces to the Beagle.

Table 3. Beagle Electrical Specification

Specification	Min	Typ	Max	Unit
Power				
Input Voltage USB		5		V
Current USB				mA
Input Voltage DC	4.8	5	5.2	V
Current DC				mA
Expansion Voltage (5V)	4.8	5	5.2	V
Current				
Expansion Voltage (1.8V)	1.75	1.8	1.85	V
Current			100	mA
USB Client				
Signal Voltage				
High Speed Mode			480	Mb/S
Full Speed Mode			12.5	Mb/S
Low Speed Mode			1.5	Mb/S
USB Host				
Output Voltage (USB)	4.8	5	5.2	V
Current		200		mA
Output Voltage (DC)	4.8	5	5.2	V
Current (based on available DC current and voltage switch)			1.5	A
Signal Voltage				
RS232				
Transmit				
High Level Output Voltage	5	5.4		V
Low Level output voltage	-5	-5.5		V
Output impedance		+/-35	+/-60	mA

Maximum data rate	250			Kbit/S
Receive				
High level Input Voltage	-2.7	-3.2		V
Lo Level Input Voltage			.4	
Input resistance	3	5	7	Kohms
JTAG				
Realview ICE Tool			30	MHz
XDS560			30	MHz
XDS510			30	MHz
Lauterbach(tm)			30	MHz
SD/MMC				
Voltage Mode 1.8V	1.71	1.8	1.89	V
Voltage Mode 3.0V	2.7	3.0		V
Current			220	mA
Clock			48	MHz
DVI-D				
Pixel Clock Frequency	25		65	MHz
High level output voltage		3.3		V
Swing output voltage	400		600	mVp-p
Maximum resolution			1024 x 768	
S-Video				
Full scale output voltage (75ohm load)	.7	.88	1	V
Offset voltage		50		mV
Output Impedance	67.5	75	82.5	Ohms
Audio In				
Peak-to-peak single-ended input voltage (0 dBFs)			1.5	Vpp
Total harmonic distortion (sine wave @ 1.02 kHz @ -1 dBFs)		-80	-75	dB
Total harmonic distortion (sine wave @ 1.02 kHz) 2 0 Hz to 20 kHz, A-weighted audio, Gain = 0 dB		-85	-78	dB
Audio Out				
Load Impedance @100 pF	14	16		ohms
Maximum Output Power (At 0.53 Vrms differential output voltage and load impedance = 16 Ohms)		17.56		mW
Peak-to-Peak output voltage			1.5	Vpp
Total Harmonic Distortion @ 0 dBFs		-80	-75	dB
Idle channel noise (20Hz to 20KHz)		-90	-85	dB

6.0 Product Contents

Under this section is a description of what comes in the box when the Beagle is purchased.

6.1 Beagle In the Box

The final packaged product will contain the following:

- 1 Box
- 1 Beagle in an ESD Bag
- 1 USB Cable
- 1 Use Disclaimer
- 1 Warranty card
- 1 RMS Form

NOTE: IN THE FINAL VERSION A SERIES OF PICTURES WILL BE PROVIDED SHOWINGTHE BOX AND ITS CONTENTS.

Figure 3. The Box

NOTE: IN THE FINAL VERSION A SERIES OF PICTURES WILL BE PROVIDED SHOWINGTHE BOX AND ITS CONTENTS.

Figure 4. Box Contents

6.2 Software on the Beagle

The board ships with U-Boot and X-Loader flashed onto the Beagle.

7.0 Beagle Hookup

This section provides an overview of all of the connectors on the Beagle and how they should be used.

7.1 Connecting USB OTG

The USB OTG port connects to the PC host and uses a miniAB connector and provided cable through which power is provided to the Beagle. If desired, the Beagle may also be connected to a self powered USB hub. **Figure 5** shows how the cable is connected to the Beagle.

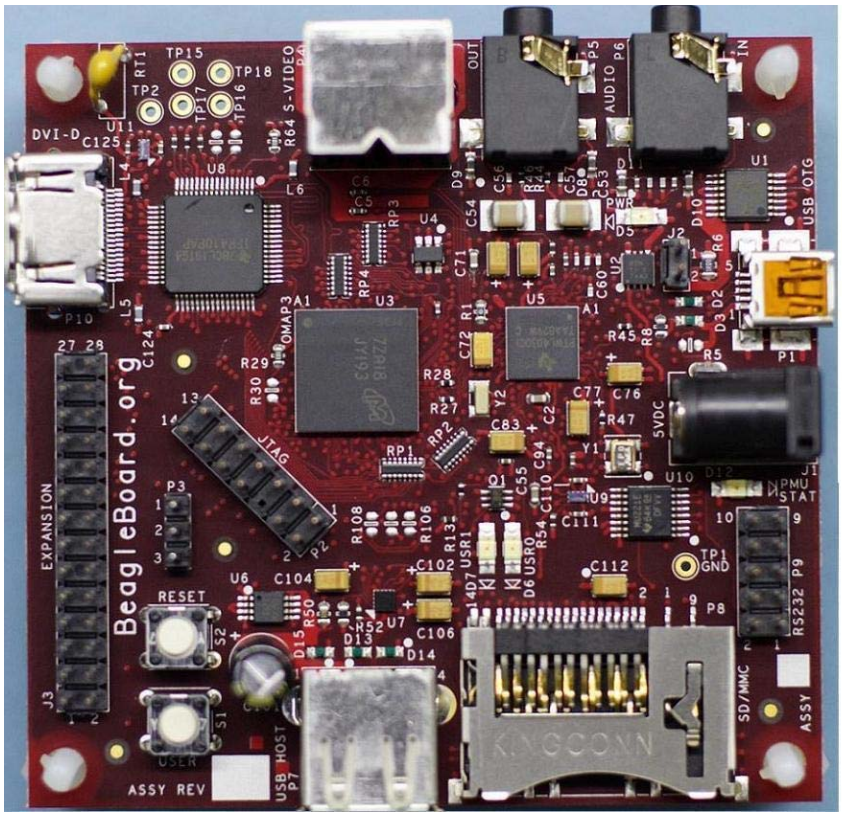

Figure 5. USB OTG Connection

7.2 Connecting Optional Power

An optional DC supply can be used to power the Beagle by plugging it into the power jack of the Beagle. The power supply is not provided with the Beagle, but can be obtained from various sources. **Figure 6** shows how to install the power supply into the power jack.

On the revision A5 Beagle, the DC connector is not provided due to a layout issue. It will be provided on Revision B boards.

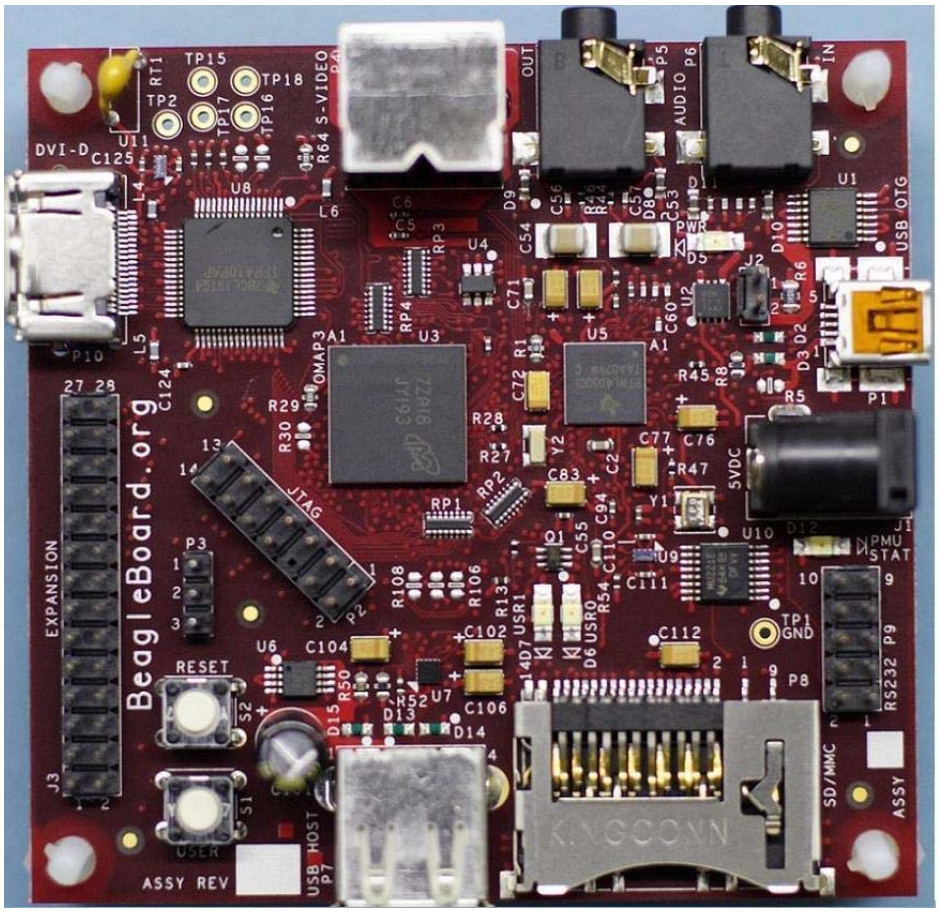

Figure 6. DC Power Connection

7.3 Connecting JTAG

A JTAG emulator can be used for advanced debugging by connecting it to the JTAG header on the Beagle. Only the 14pin version of JTAG is supported. If a 20pin version is needed, contact your emulator supplier for the appropriate adapter. **Figure 7** shows the proper connection of the **JTAG** cable to the Beagle.

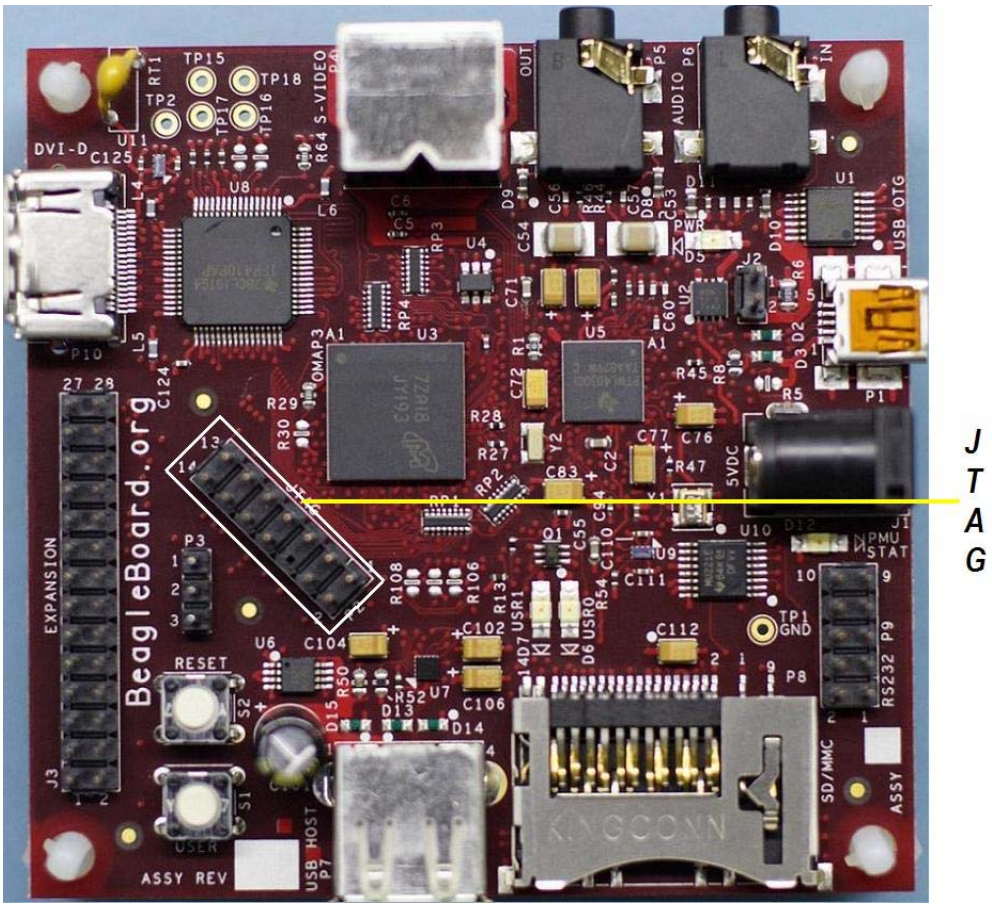

Figure 7. Beagle JTAG Connection

7.4 Connecting Serial Cable

In order to access the serial port of the Beagle a flat cable is required. This can then be used to connect to a PC. The adapter will not plug directly into the PC and will require an external Female to Female twisted cable in order to connect it to the PC. The ribbon cable is not supplied with the Beagle but can be obtained form numerous sources. **Figure 8** shows how the ribbon cable is to be installed.

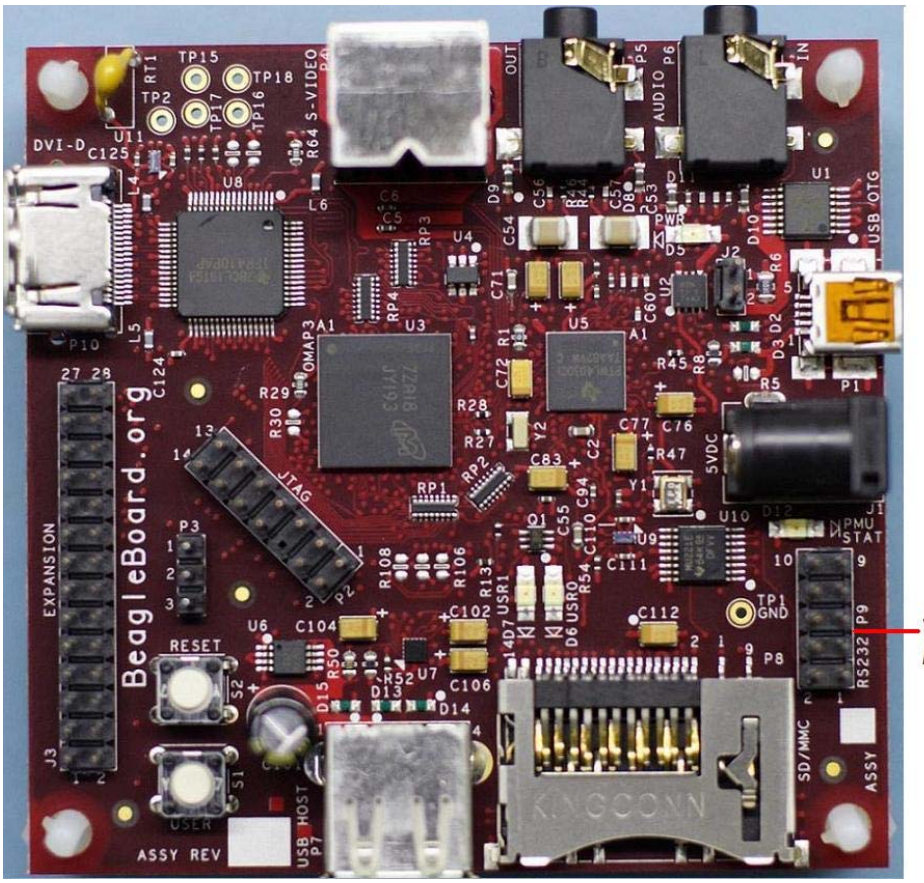

Figure 8. Beagle Serial Cable Connection

7.5 Connecting S-Video

An S-Video cable can be connected to the Beagle. From there is can be connected to a TV or monitor that supports an S-Video input. **Figure 9** shows the proper connection of the S-Video cable.

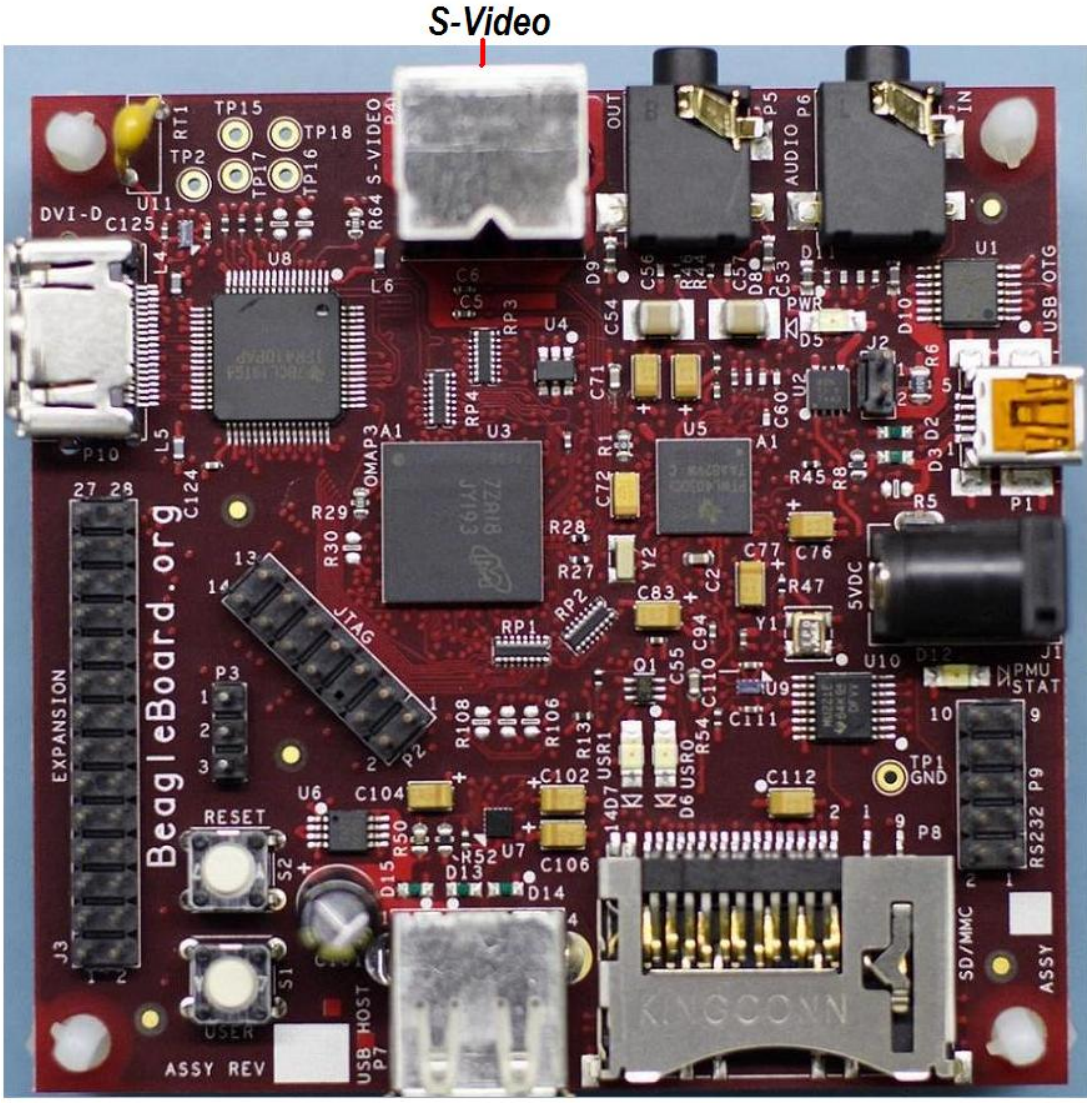

Figure 9. Beagle S-Video Connection

7.6 Connecting DVI-D Cable

In order to connect the DVI-D output to a monitor, a HDMI to DVI-D cable is required. This cable is not supplied with Beagle but can be obtained through numerous sources. **Figure 10** shows the proper connection of the HDMI cable.

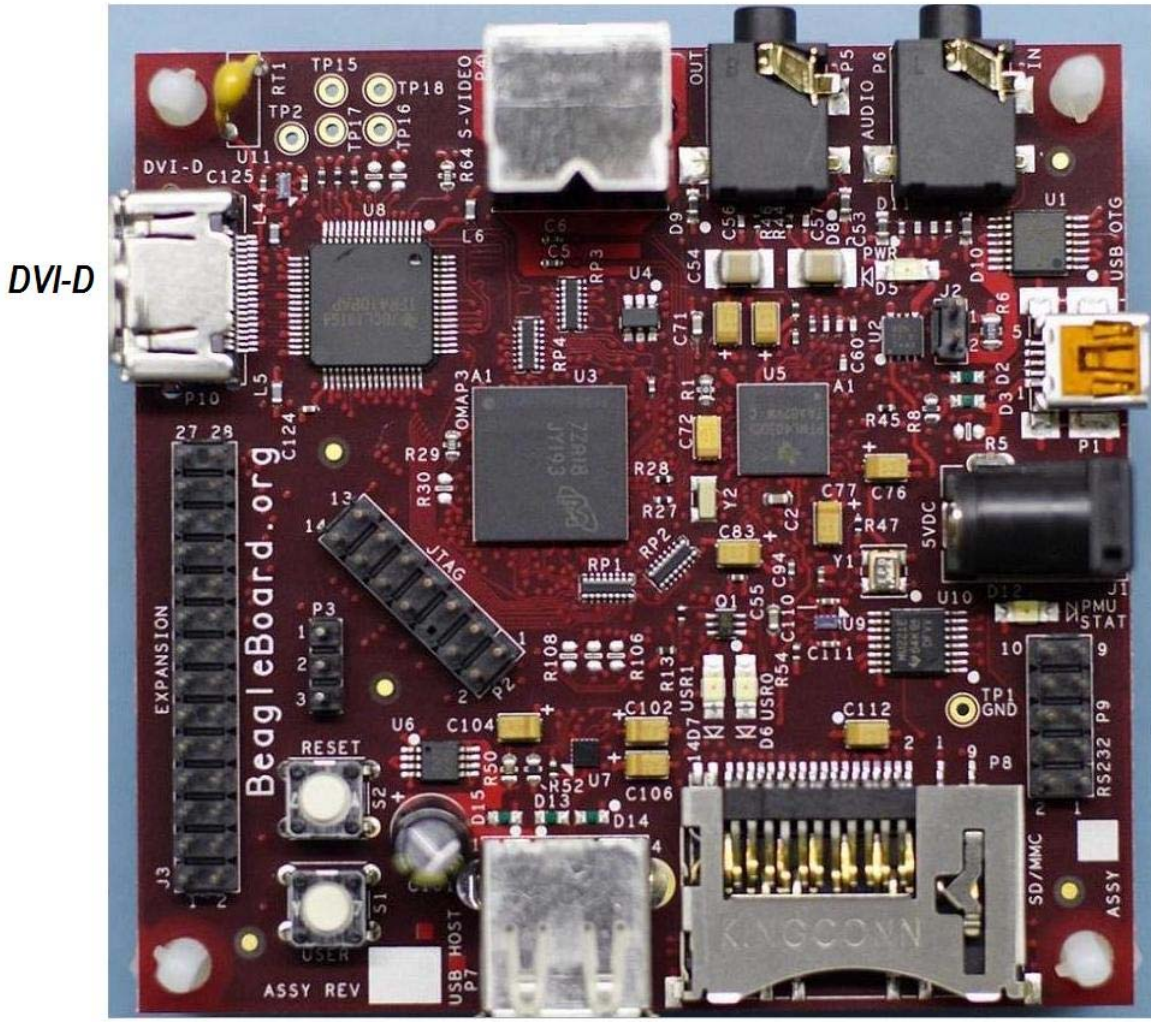

Figure 10. Beagle DVI-D Connection

7.7 Connecting USB Host Cable

A USB device or external hub can be connected to the USB Host port on the Beagle which provides a Type A Female connector, the same you would find on a PC or USB hub. If a hub is used, it should be a self powered version. The host port on Beagle will supply power, but it will be limited to the power that is left from what the Beagle will consume. A cable is not provided with Beagle, but can be obtained form numerous sources if needed. **Figure 11** shows the connection of the USB host interface using a thumb drive. There is sufficient power to power a thumb drive with the need for external power.

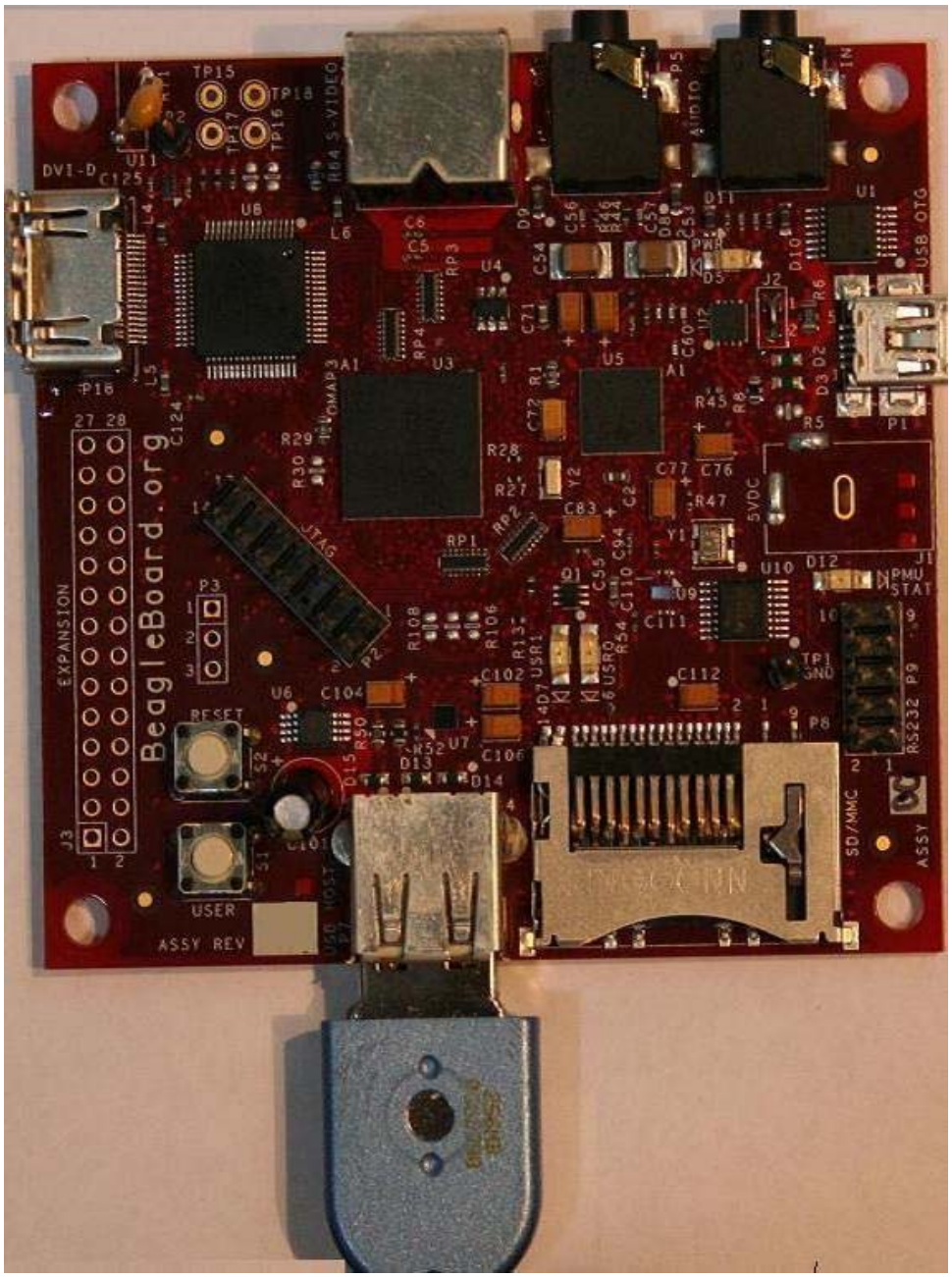

Figure 11. Beagle USB Host Connection

7.8 Connecting Stereo Out Cable

External Audio output device can be connected to the Beagle. External stereo powered speakers can be connected to the Audio out port. A standard 3.5mm jack is provided for the connectivity. The audio cables are not provided with Beagle, but can be obtained from just about anywhere. **Figure 12** shows how the cable connected to the stereo out jack.

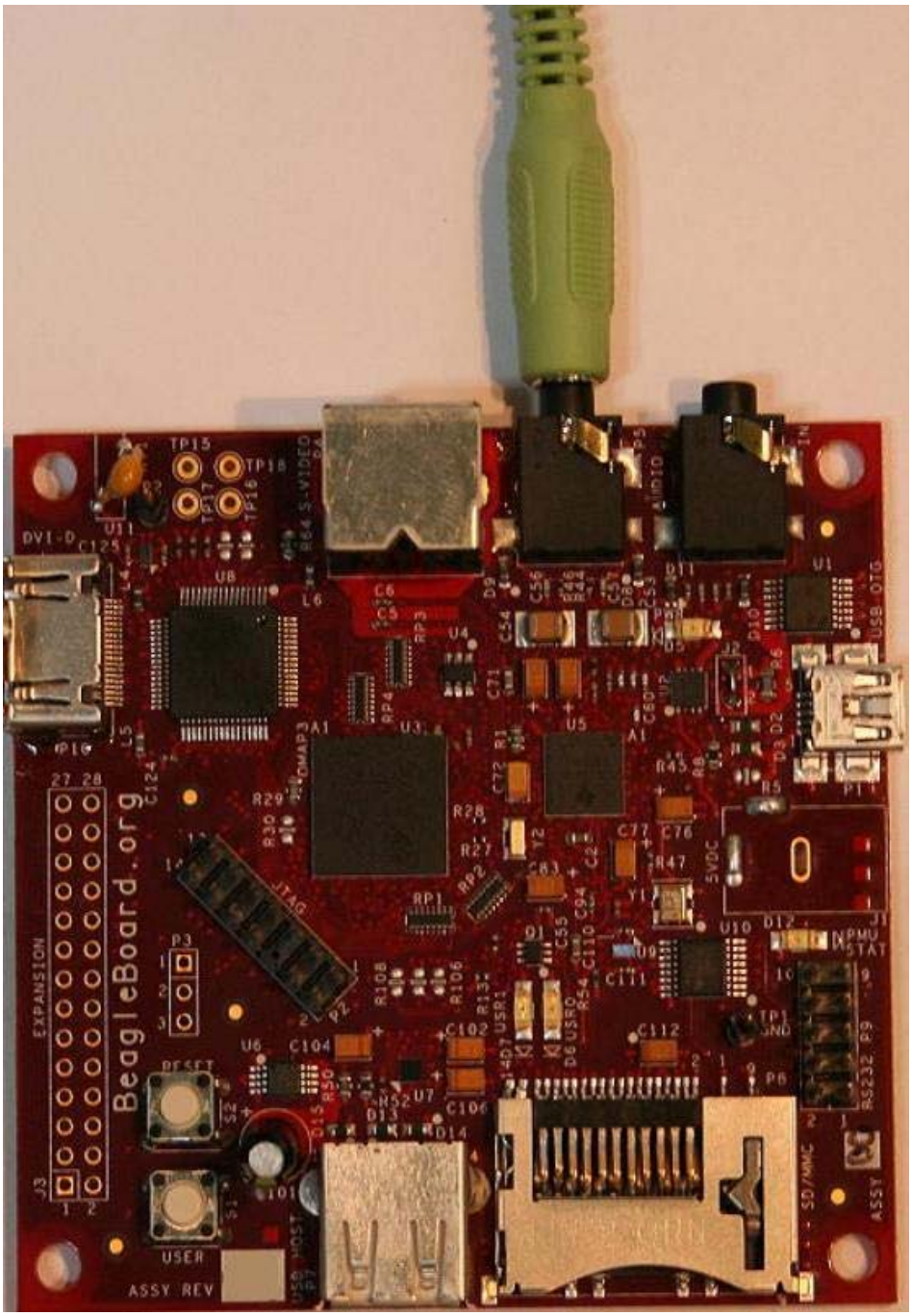

Figure 12. Beagle Audio Cable Connection

7.9 Connecting Stereo In Cable

External Audio input devices can be connected to the Beagle. This can be the audio out put of a stereo or PC. A standard 3.5mm jack is provided for the connectivity. The audio cables are not provided with Beagle, but can be obtained from just about any source. **Figure 13** shows how the cable is connected to the stereo input jack.

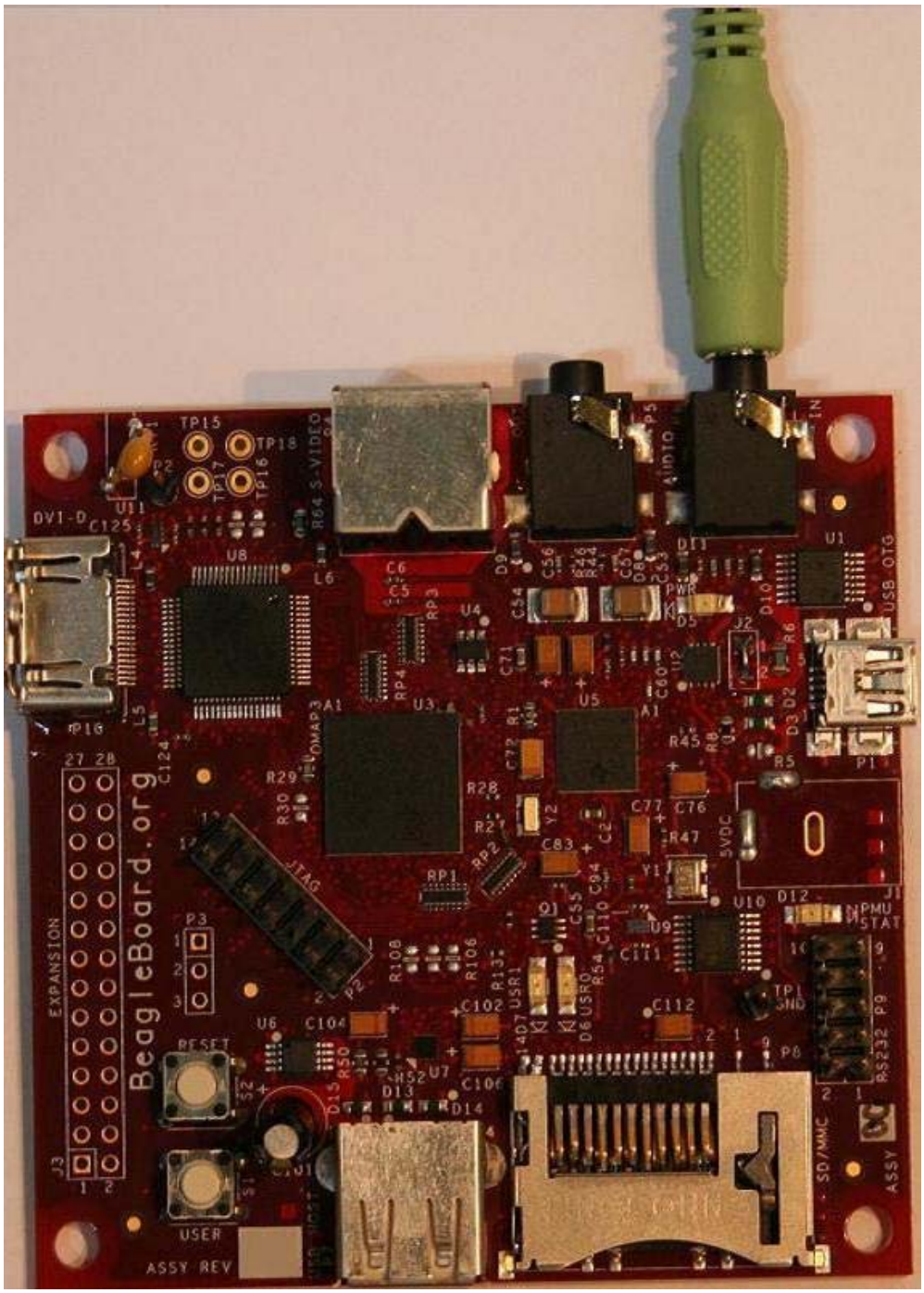

Figure 13. Beagle Audio Cable Connection

7.10 Indicator Locations

There are four green indicators on the Beagle. One of them, POWER, indicates that the main supply is active. The other three can be controlled by the software. **Figure 14** shows the location of each indicator.

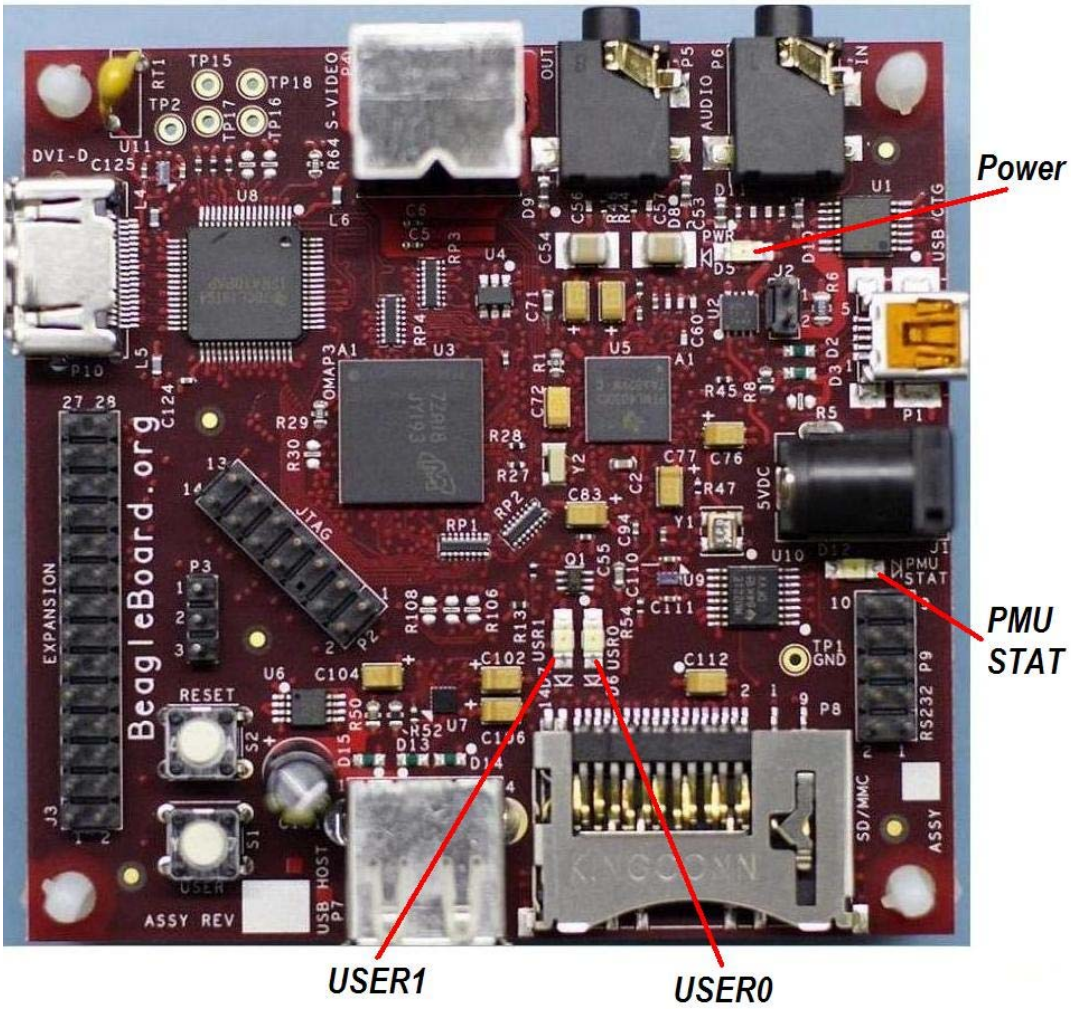

Figure 14. Beagle Indicator Location

7.11 Button Locations

There are two buttons on the Beagle. The **RESET** button when pressed will force a full board reset. The **USER** button is used by the SW for user interaction. If the user holds the **USER** button down while pressing and releasing the **RESET** button, the Beagle will enter the ROM boot loader mode. **Figure 15** shows the location of the buttons.

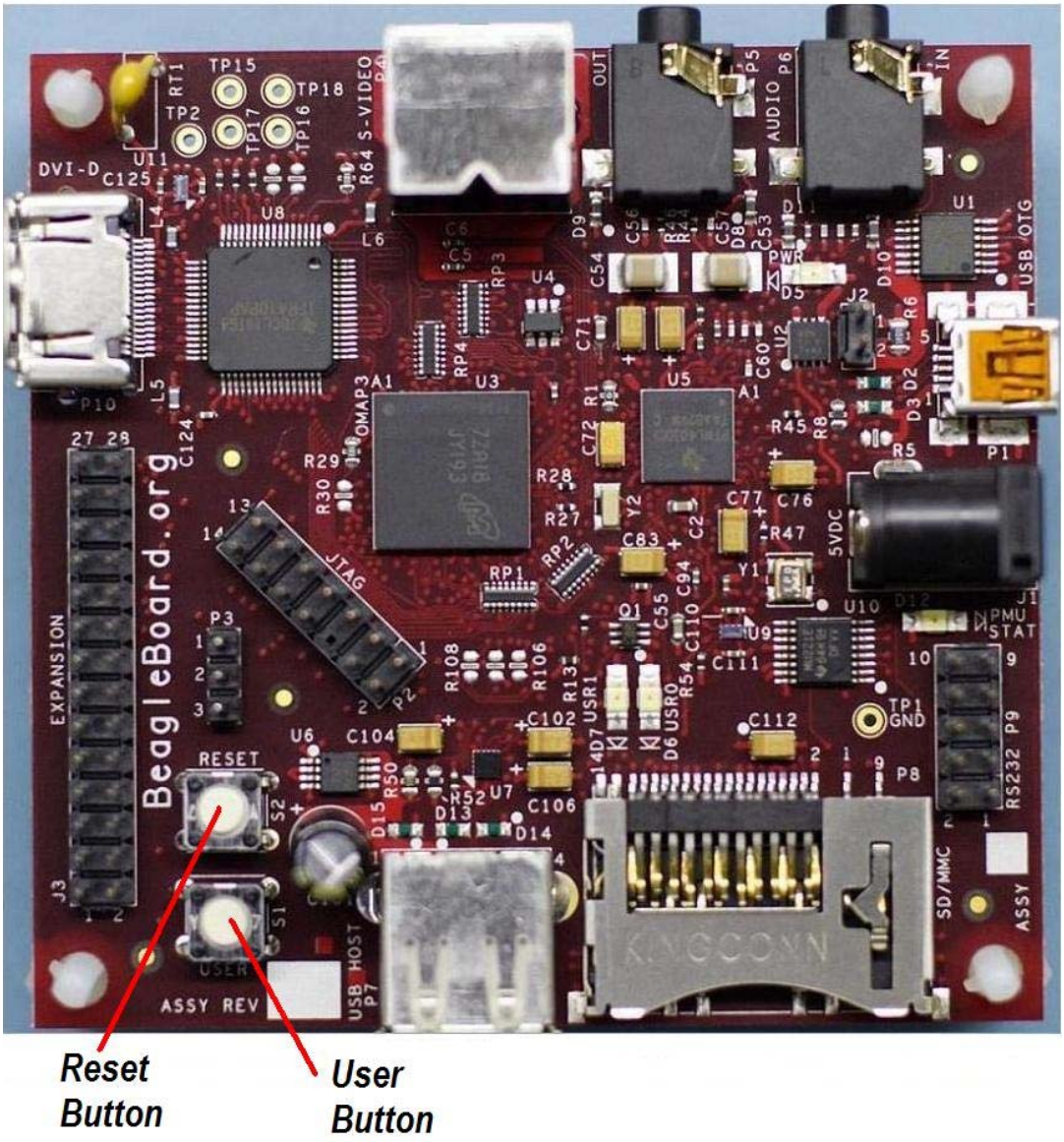

Figure 15. Beagle Button Location

7.12 SD/MMC Connection

The SD/MMC connector can be used for Memory or SDIO type cards. This is a full size connector and will support various cards. Whether a particular card is supported or not, is dependent on the available SW drivers. **Figure 16** shows the location of the SD/MMC card and the orientation of the card.

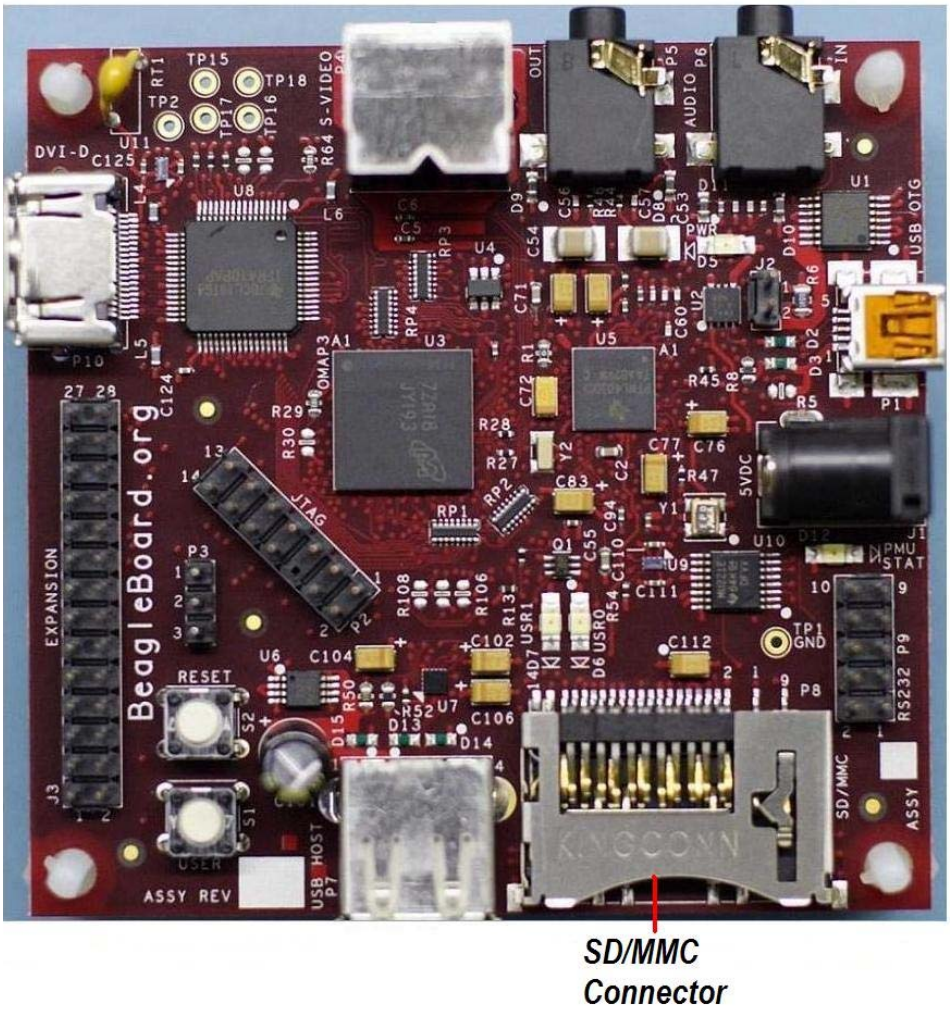

Figure 16. Beagle SD/MMC Location

8.0 Beagle System Architecture and Design

This section provides a high level description of the design of the Beagle and its overall architecture.

8.1 System Block Diagram

Figure 17 is the high level block diagram of the Beagle. If you will notice, the block diagram is configured to match the component placement of the Beagle.

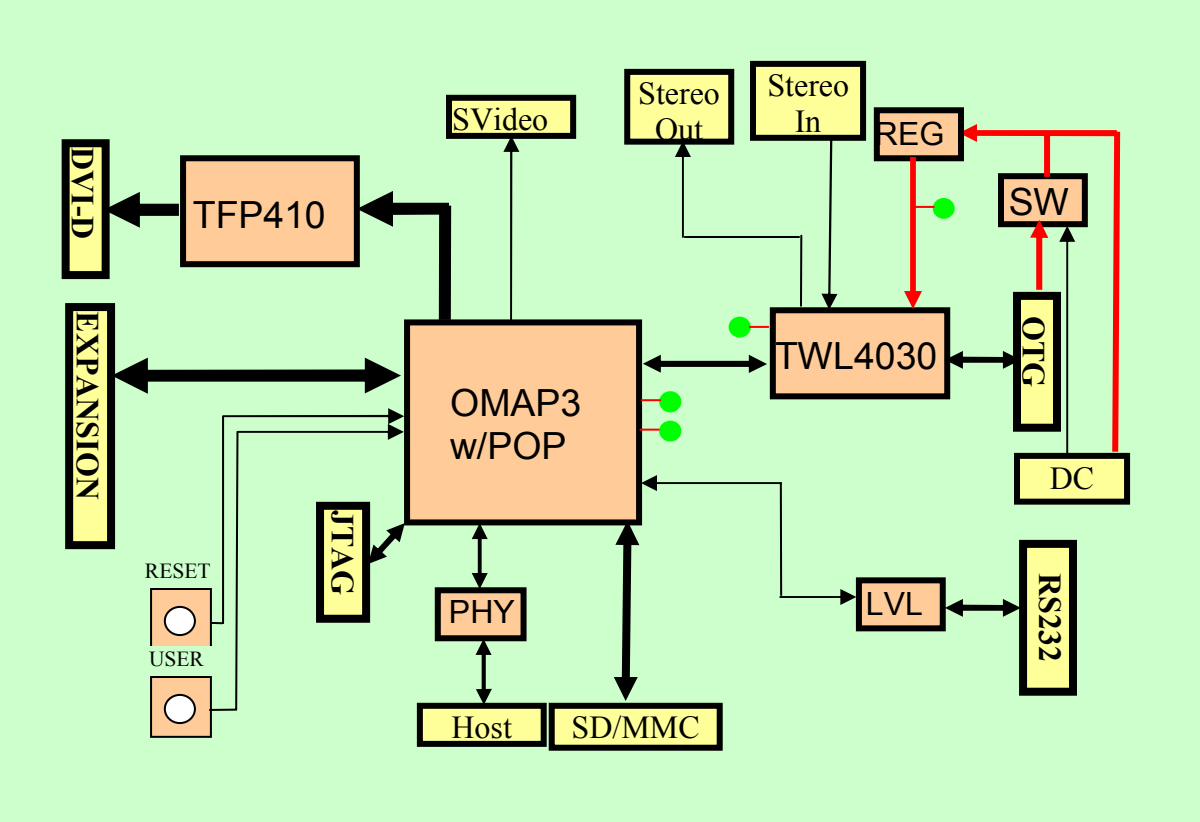

Figure 17. Beagle High Level Block Diagram

Figure 18 shows the location of the components as shown in the block diagram and is of the full assembly. The expansion and DC connectors are not provided on the Revision A version of the Beagle. The Revision B version will contain the DC connector

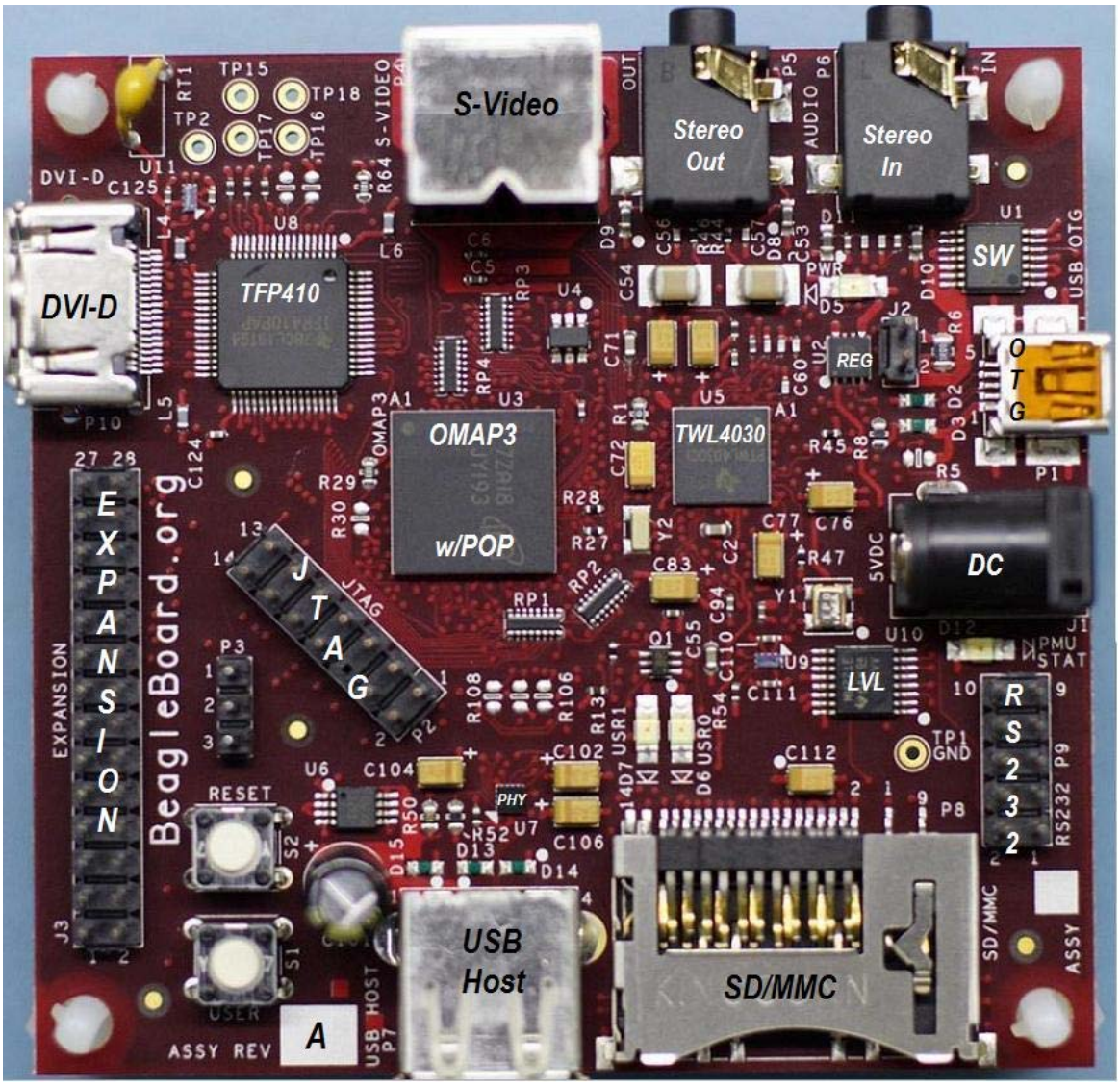

Figure 18. Beagle Top Side Components

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There are no key components on the back of the Beagle, but **Figure 19** has been provided for completeness.

Figure 19. Beagle Backside Components

This remainder of this section describes in detail the architecture and design of the Beagle.

You will notice certain things in this section.

- The schematic has been created for each section showing only the pertinent components and their connections.
- The pin names differ from the actual schematic. For ease of reading, the names have been truncated to only show the specific functions of that pin as used in the design.

8.2 Input Power

There are two possible sources of the 5V required by the Beagle. It can come from the USB OTG port connected to a PC, powered USB HUB, or a 5V DC supply. The USB supply is sufficient to power the Beagle. However, depending on the load needed by the USB Host port on Beagle, additional power may be required. This is where the DC supply comes in to play. You will be able to use the USB connection while running from the DC supply.

It should also be noted that if an OTG configuration is used, for example tying two Beagles together via a UBS OTG cable, both of the Beagles must be powered by the DC supply.

Figure 20 is the design of the power input section.

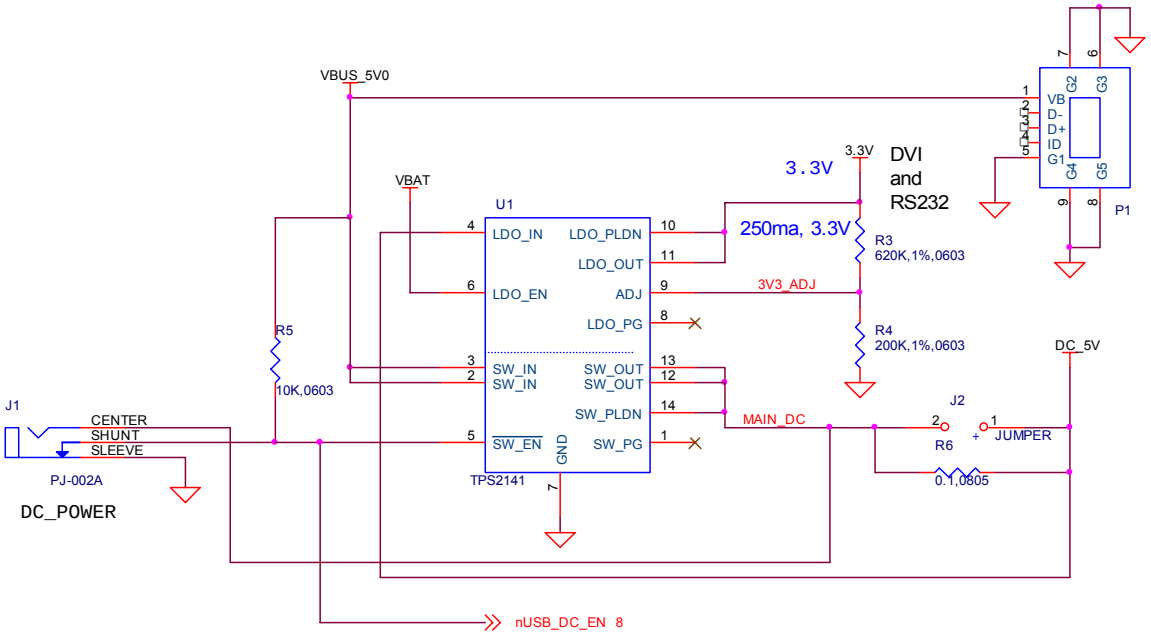

Figure 20. Input Power Section

8.2.1 USB DC Source

The USB specification requires that the current consumed prior to enumeration be limited to 100mA @ 5V (500mW). The 5V DC from the USB is routed through the **TPS2141** switch to insure that this requirement is met. The **TPS2141** is a USB 2.0 Specification-compatible IC containing a dual-current limiting power switch and an adjustable low dropout regulator (LDO). Both the switch and LDO limit inrush current by controlling the turn on slew rate. The dual-current-limiting feature of the switch allows USB peripherals to utilize high-value capacitance at the output of the switch, while keeping the inrush current low.

During turn on, the switch limits the current delivered to the capacitive load to less than 100 mA. When the output voltage from the switch reaches about 93% of the input voltage, the switch power good output goes high, and the switch current limit increases to 800mA (minimum), at which point higher current loads can be turned on. The higher current limit provides short circuit protection while allowing the peripheral to draw maximum current from the USB bus.

8.2.2 Wall Supply Source

A wall supply can be used to provide power to the board. A regulated 5V DC supply of at least 500mA is required. It needs to have a 2.1mm plug with a center hot configuration.

In the event that a higher DC load is required due either to the addition of a Daughtercard or higher current device on the USB host port, a higher current supply can be used. The maximum current should not exceed 2A.

On the revision A5 Beagle, the DC connector is not provided due to a layout issue. It will be provided on Revision B board.

8.2.3 DC Source Control

Unlike when powering from the USB port, in the case of the DC voltage, the current limiting is not required. As long as the DC supply is not connected, the switch for the USB is enabled. When the DC supply is plugged in, the switch is disabled because the ground is removed from **pin 5** of the **TPS2141**. This insures that the 5V from the USB is not connected. In the case where there is no USB plugged in, there is no 5V available to be routed so the removal of the pullup in **pin 5** has no affect.

8.2.4 3.3V Supply

The **TPS2141** has an integrated 3.3V LDO. This is being used to supply the **3.3V** as required on the Beagle for the **DVI-D** interface and the **UART**. The input to the LDO is supplied by the main **DC_5V**. This insures that the power to the LDO can be supplied by either the USB or the DC wall supply and that the current measurement includes the 3.3V supply.

8.2.5 Current Measurement

Jumper **J2** is a set of pads that can facilitate the installation of a .1 x .1 header. This allows for the voltage drop across the resistor to be measured, providing a way to measure the current consumption of the Beagle from the main voltage rails, either USB

or DC. The resistor, **R6**, is a .1 ohm resistor across which the voltage is measured. The reading you get is .1mV per mA of current.

8.3 Power Conditioning

This circuitry regulates the DC input to a nominal 4.2VDC level. This is required in order to meet the maximum DC voltage level as specified by the TWL4030 Power Management device.

Figure 21 is the power conditioning section of the Beagle.

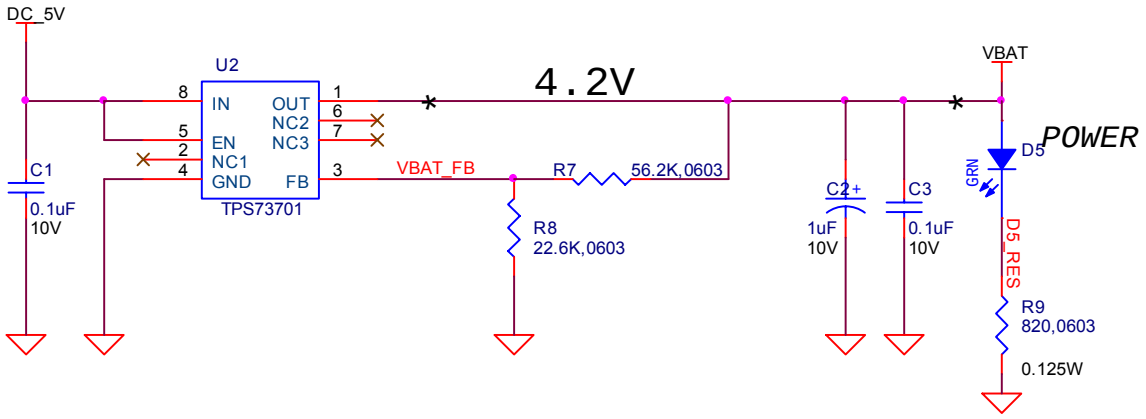

Figure 21. Power Conditioning

The **TWL4030** provides the main power rails to the board. It has a maximum limit of 4.8V on its VBAT input and a nominal of 4.2V. **U2**, the **TPS73701**, is used to convert the DC_5V, which can come from a DC wall supply or the USB, to 4.2V to meet this requirement. The **TPS737701** is a linear low-dropout (LDO) voltage regulator and is thermal shutdown and current limit protected. It has the ability to deliver 1A of current, although this is far and above the requirements of the board. By adjusting **R7** and **R8**, the actual voltage can be adjusted if needed.

The LED **D5** is an indication that the 4.2V is present.

8.4 TWL4030 Reset and Power Management

The **TWL4030** supplies several key functions on the Beagle. This section covers a portion of those functions centered on the power and reset functions. Included in this section is:

- Main Core Voltages
- Peripheral Voltages

- Power Sequencing
- Reset
-

The other functions are covered in other sections in this document and are grouped by their overall board functions. The explanation of the various regulators found on the TWL4030 is based upon how they are used in the board design and are not intended to reflect the overall capability of the TWL4030 device. Please refer to the TWL4030 documents for a full explanation of the device operation.

8.4.1 Main Core Voltages

The **TWL4030** supplies the three main voltage rails for the **OMAP3** processor and the board:

- VOCORE_1V3 (1.2V)
- VDD2 (1.3V)
- VIO_1V8 (1.8V)

The **VOCORE_1V3** defaults to **1.2V** at power up, but can be adjusted by software to the **1.3V** level. **Figure 22** is the interfacing of the TWL4030 to the system as it provides the three main rails.

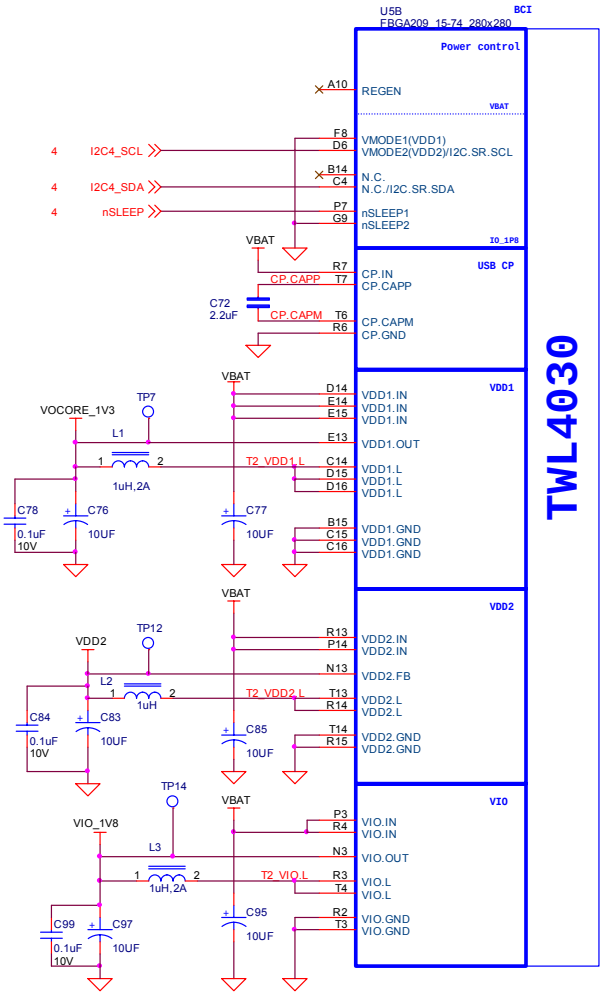

Figure 22. Main Core Voltages

8.4.2 Main DC Input

The main supply to the **TWL4030** for the main rails is the **VBAT** rail which is a nominal 4.2V. Each rail has a filter cap of **10uF** connected to each of the three inputs. A **.1uF** cap is also provided for high frequency noise filtering.

8.4.3 OMAP3 I2C Control

The various components in the TWL4030 are controlled from the OMAP3 via the I2C interface.

Figure 23. OMAP3 Control Interface

8.4.4 Smart Reflex

VDD1 and **VDD2** regulators on the **TWL4030** provide SmartReflex-compliant voltage management. The SmartReflex controller in the **OMAP3** interfaces with the **TWL4030** counterpart through the use of a dedicated **I2C** bus. The **OMAP3** computes the required voltage and informs the **TWL4030** using the SmartReflex I2C interface. **Figure 22** shows the connection of the I2C2 control interface for SmartReflex to the OMAP3.

SmartReflex control of the **VDD1** and **VDD**2 regulators can be enabled by setting the SMARTREFLEX_ENABLE bit (DCDC_GLOBAL_CFG[3]) to 1. To perform **VDD1** voltage control through the SmartReflex interface, the TWL4030 provides the VDD1_SR_CONTROL register. The MODE field of the VDD1_SR_CONTROL register can be set to 0 to put VDD1 in an ACTIVE state; setting the field to 1 moves **VDD1** to a SLEEP state. **VDD1** output voltage can be programmed by setting the VSEL field of the VDD1_SR_ CONTROL register. The **VDD1** output voltage is given by VSEL*12.5 mV + 600 mV.

8.4.5 VOCORE_1V3

The **VOCORE_1V3** rail is supplied by the **VDD1** regulator of the **TWL4030**. The **VDD1** regulator is a 1.1A stepdown power converter with configurable output voltage between 0.6 V and 1.45 V in steps of 12.5 mV. This regulator is used to power the **OMAP3** core.

The **OMAP3** can request the **TWL4030** to scale the **VDD1** output voltage to reduce power consumption. The default output voltage at power-up depends on the boot mode settings, which in the case of the Beagle is 1.2V. The output voltage of the **VDD1** regulator can be scaled by software or hardware by setting the ENABLE_VMODE bit (VDD1_VMODE_CFG[0]). In each of these modes, the output voltage ramp can be single-step or multiple-step, depending on the value of the STEP_REG field of the VDD1_STEP[4:0] register. The VOCORE_1V3 rail should be set to 1.3V after boot up.

Apart from these modes, the **VDD1** output voltage can also be controlled by the **OMAP3** through the SmartReflex I2C interface between the host processor and the **TWL4030**. The default voltage scaling method selected at reset is a software-controlled mode. Regardless of the mode used, **VDD1** can be configured to the same output voltage in sleep mode as in active mode by programming the DCDC_SLP bit of the VDD1_VMODE_CFG[2] register to 0. When the DCDC_SLP bit is 1, the sleep mode output voltage of **VDD1** equals the floor voltage that corresponds to the VFLOOR field (VDD1_VFLOOR[6:0]).

8.4.6 VDD2

The **VDD2** voltage rail is generated by the **TWL4030** using the **VDD2** regulator. The **VDD2** regulator is a stepdown converter with a configurable output voltage of between 0.6 V and 1.45 V. This regulator is used to power the OMAP3 core. **VDD2** differs from **VDD1** in its current load capabilities with an output current rating of 600 mA in active mode.

The **VDD2** provides different voltage regulation schemes. When **VDD2** is controlled by the VMODE2 signal or with the SmartReflex interface, the range of output voltage is 0.6 V to 1.45 V. The use of the VMODE2 signal and the VDD2_VMODE_CFG, VDD2_STEP, VDD2_FLOOR, and VDD2_ROOF registers is similar to the use of the corresponding signals and registers for **VDD1**. **VDD2** shares the same SmartReflex I2C bus to provide voltage regulation. The VDD2_SR_CONTROL register is provided for controlling the **VDD2** output voltage in SmartReflex mode.

When the **VDD2** is used in software-control mode, the VSEL (VDD2_ DEDICATED[4:0]) field can be programmed to provide output voltages of between 0.6 V and 1.45 V. The output voltage for a given value of the VSEL field is given by VSEL*12.5 mV + 600 mV. If the VSEL field is programmed so that the output voltage computes to more than 1.45 V, the TWL4030 sets the **VDD2** output voltage to 1.5 V.

8.4.7 VIO_1V8

The **VIO_1V8** rail is generated by the TWL4030 VIO regulator. The VIO output is a stepdown converter with a choice of two output voltage settings: 1.8 V or 1.85 V. The voltage is set by configuring the VSEL bit (VIO_VSEL[0]). When the VSEL bit is set to 0, the output voltage is 1.8 V, and when it is set to 1, the output voltage is 1.85 V.

When the **TWL4030** resets, the default value of this LDO is 1.80 V; the OMAP3 must write 1 to the VSEL field to change the output to 1.85 V. The default for the Beagle is 1.8V. This regulator output is used to supply power to the system memories and I/O ports. It is one of the first power supplies to be switched on in the power-up sequence. VIO does not support the SmartReflex voltage control schemes. VIO can be put into sleep or off mode by configuring the SLEEP_STATE and OFF_STATE fields of the VIO_REMAP register.

8.5 Peripheral Voltages

There are five additional voltages used by the system that are generated by the **TWL4030**. These are:

- VDD_PLL2
- VDD_PLL1
- VDAC_1V8
- VDD_SIM

- VMMC1

Figure 24 shows the peripheral voltages supplied by the **TWL4030**.

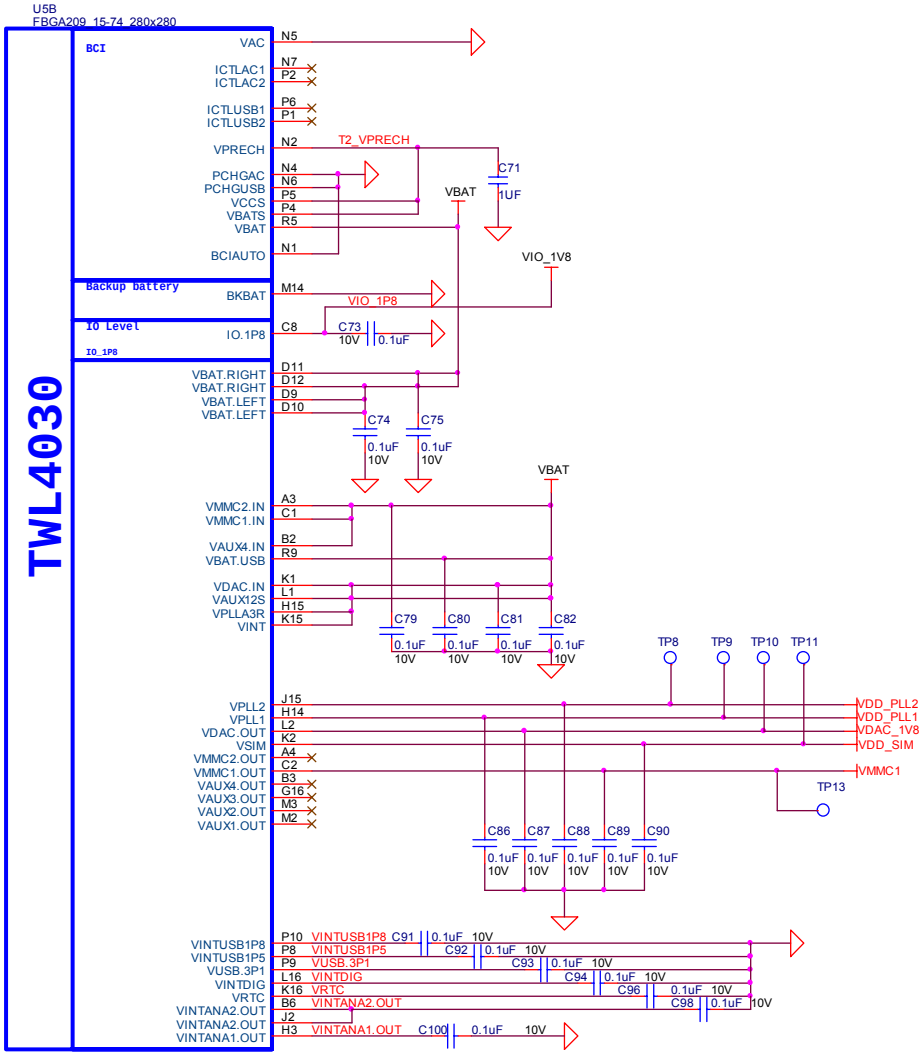

Figure 24. Peripheral Voltages

8.5.1 VDD_PLL2

This programmable LDO is used to power the OMAP3 PLL circuitry. The **VPLL2** LDO can be configured through the I2C interface to provide output voltage levels of 1.0 V, 1.2 V, 1.3 V, or 1.8 V, based on the value of the VSEL field (VPLLI_DEDICATED[3:0]). On the board this rail is used to power DVI output for pins DSS_DATA(0:5), DSS_DATA(10:15) and DSS_DATA(22:23). The VPLL2 must be set to 1.8V for proper operation of the **DVI-D** interface.

8.5.2 VDD_PLL1

The VPLL1 programmable LDO regulator is low-noise, linear regulator used for the OMAP3 PLL supply. The VDD_PLL1 rail is initialized to 1.8V.

8.5.3 VDAC_1V8

The **VDAC** programmable LDO regulator is a high-PSRR, low-noise, linear regulator that powers the OMAP3 dual-video DAC. It is controllable with registers via I2C and can be powered down if needed. The **VDAC** LDO can be configured to provide 1.2V, 1.3 V, or 1.8 V in on power mode, based on the value of the VSEL field (VDAC_DEDICATED[3:0]). The VDAC_1V8 rail should be set to 1.8V for the Beagle.

8.5.4 VDD_SIM

This voltage regulator is a programmable, low dropout, linear voltage regulator supplying the bottom 4 bits of the 8 bit **SD/MMC** card slot. The VSEL field (VSIM_DEDICATED[3:0]) can be programmed to provide output voltage of 1.0 V, 1.2 V, 1.3 V, 1.8 V, 2.8 V, or 3.0 V and can deliver up to 50mA. The default output voltage of this LDO as directed by the **TWL4030** boot pins is 1.8V.

8.5.5 VMMC1

The **VMMC1** LDO regulator is a programmable linear voltage converter that powers the MMC1 slot. It includes a discharge resistor and overcurrent protection (short-circuit). This LDO regulator can also be turned off automatically when the MMC card extraction is detected. The VMMC1 LDO is powered from the main **VBAT** rail. The **VMMC1** rail defaults to 3.0V as directed by the **TWL4030** boot pins and will deliver up to 220mA. It can be set to 1.8V in the event 3V cards are being used.

8.5.6 Boot Configuration

The boot configuration pins on the **TWL4030** determine the power sequence of the device. For the OMAP3 support, the boot pin configuration is fixed at:

- **Boot0** tied to VBAT
- **Boot1** tied to Ground.

8.5.7 Power Sequencing

Based on the boot configuration pins, the **TWL4030** knows the type of OMAP processor that it needs to support, in this case the OMAP3. The voltages are ramped in a sequence that is compatible with the OMAP3 processor. **Figure 25** is the sequence that the power rails, clocks, and reset signal come up.

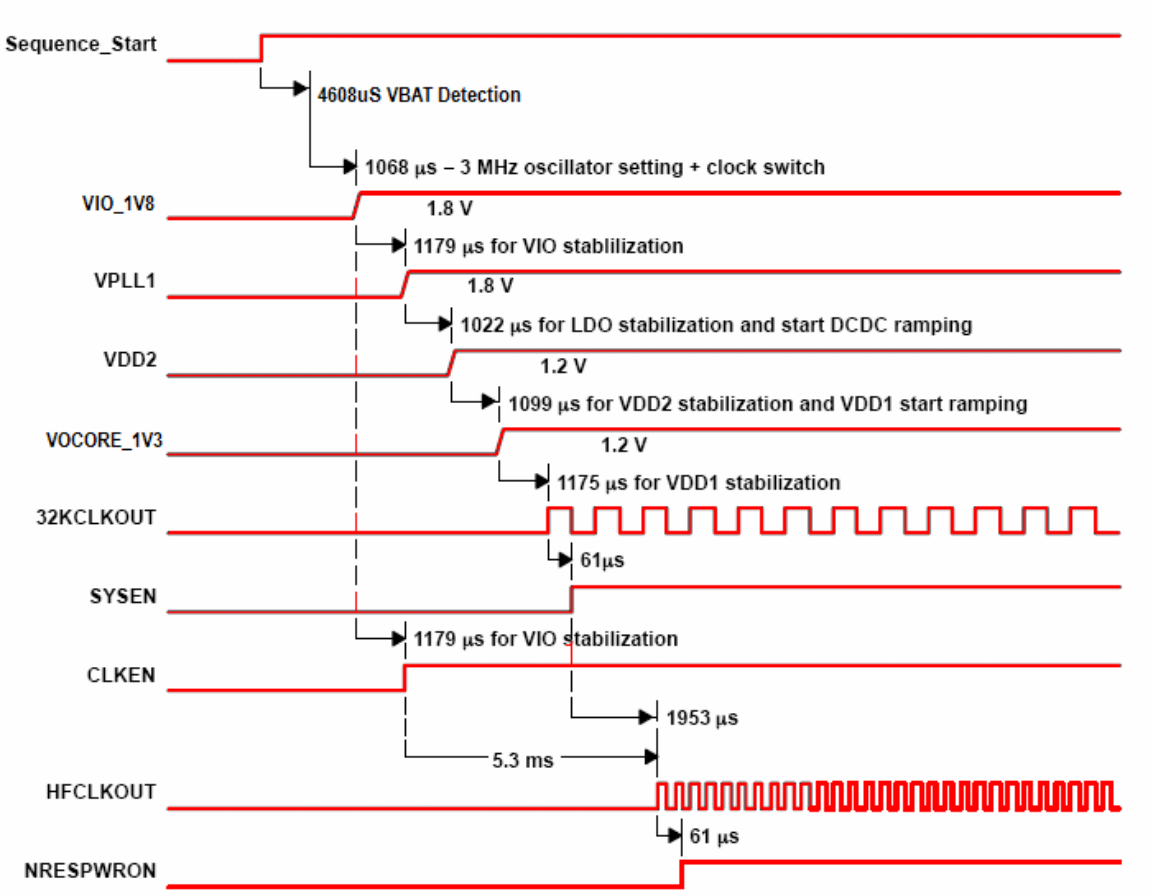

Figure 25. Power Sequencing

8.5.8 Reset Signals

The Beagle uses two distinct reset circuits:

- Warm Reset
- Cold Reset

Figure 26 shows the connections for the Warm and Cold Reset.

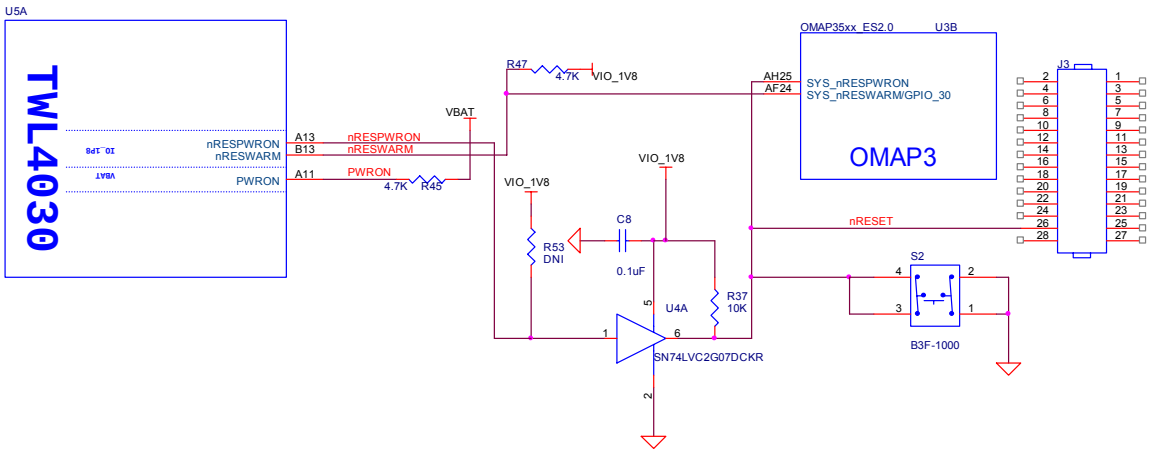

Figure 26. Reset Circuitry

8.5.8.1 Warm Reset

The warm reset is generated by the **OMAP3** processor on power up. The **nRESWARM** signal is a bidirectional reset. When an internal reset occurs, **nRESWARM** goes low and resets all the peripherals and the **TWL4030**. The **TWL4030** can be configured to perform a warm reset of the device to bring it into a known defined state by detecting a request for a warm reset on the **NRESWARM** pin. The minimum duration of the pulse on the **nRESWARM** pin should be two 32-kHz clock cycles.

The **nRESWARM** output is open-drain; consequently, an external pullup resistor is required. There is no way for the user to generate a warm reset on the Beagle.

8.5.8.2 Cold Reset

On power up as shown in **Figure 24**, the **TWL4030** generates **nRESPWRON**, power on reset. The signal from the **TWL4030** is an output only and is not an open drain signal. By running the signal through a buffer, **SN74LVC2G07**, the signal becomes open drain, which requires a pullup on the signal. This will allow the **nRESPWRON** signal to be pulled low, by pressing the reset switch **S2**, to force a reset to the **OMAP3** processor and to any device on the expansion card that require a reset.

It also allows for the reset signal to be pulled low or held low for an extended time by circuitry on the expansion card if needed.

8.5.8.3 PWRON

You will notice another signal on the **TWL4030** called **PWRON**. This signal is referenced in the **TWL4030** documentation. In the Beagle design it is not used but it is pulled high to insure the desired operation is maintained.

8.6 OMAP3 Processor

The heart of Beagle is the OMAP3 processor. **Figure 27** is a high level block diagram of the OMAP3.

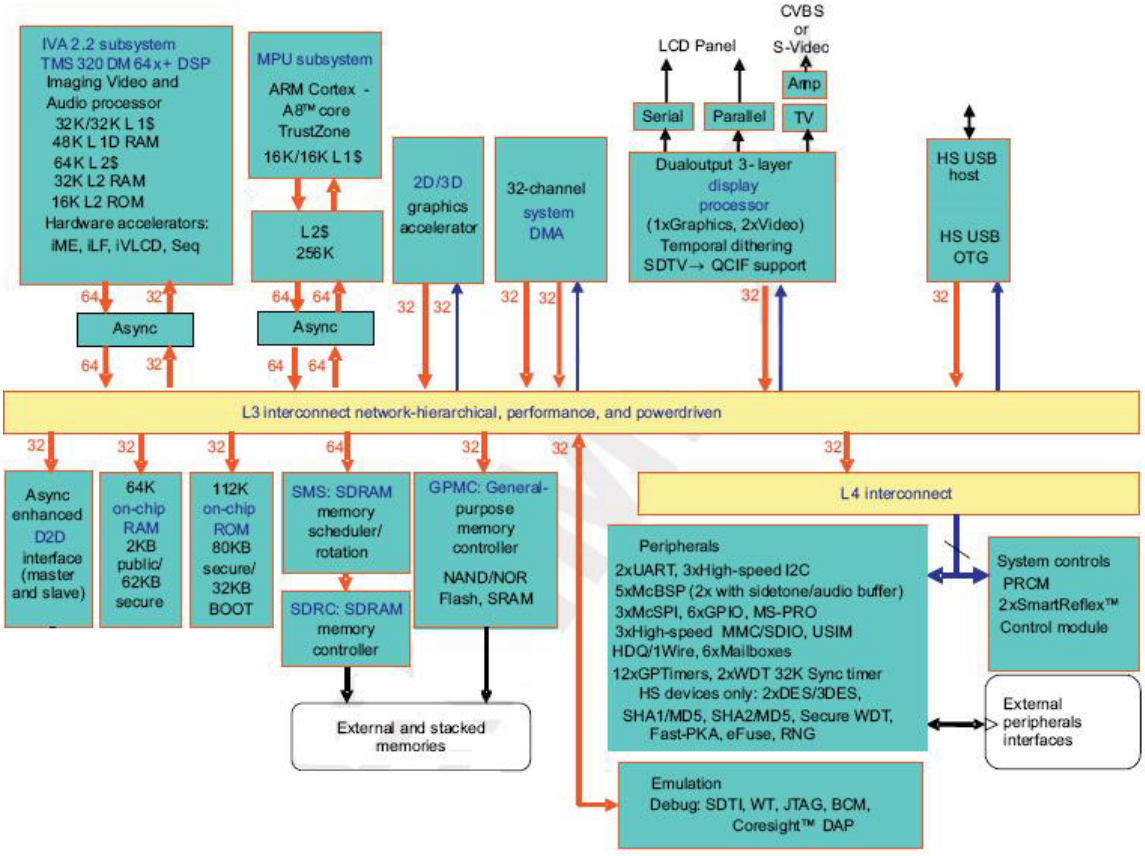

Figure 27. OMAP3 Block Diagram

8.6.1 Overview

The OMAP3 high-performance, multimedia application device is based on the enhanced OMAP™ 3 architecture and is integrated on TI's advanced 65-nm process technology. The OMAP3 architecture is configured with different sets of features in different tier devices. Some features are not available in the lower-tier devices. For more information, refer to the OMAP3 Technical Reference Manual (TRM).The architecture is designed to provide best-in-class video, image, and graphics processing sufficient to various applications.

The OMAP3 supports high-level operating systems (OSs), such as:

- Windows CE
- Linux
- Others

This OMAP3 device includes state-of-the-art power-management techniques required for high-performance low power products.
The OMAP3 supports the following functions and interfaces on the Beagle:

- Microprocessor unit (MPU) subsystem based on the ARM Cortex-A8™ microprocessor
- POP Memory interface
  - 1Gb MDDR (128Mbytes)
  - 2Gb NAND Flash (256 Mbytes)
- 24 Bit RGB Display interface (DSS)
- SD/MMC interface (2)
- USB OTG interface
- USB HS Host interface
- NTSC/PAL/S-Video output
- Power management
- Serial interface
- I^2C interface
- I^2S Audio interface (McBSP2)
- Expansion McBSP1
- JTAG debugging interface

8.6.2 SDRAM Bus

The SDRAM bus is not accessible on the Beagle. Its connectivity is limited to the POP memory access on the top of the OMAP3 and therefore is only accessible by the SDRAM memory.

The base address for the DDR SDRAM in the POP device is **0x8000 0000**.

8.6.3 GPMC Bus

The GPMC bus is not accessible on the Beagle. Its connectivity is limited to the POP memory access on the top of the OMAP3 and therefore is only accessible by the NAND memory.

The memory on the GPMC bus is NAND and therefore will support the classical NAND interface. The address of the memory space is programmable. Please consult the Software Reference for more information.

8.6.4 DSS Bus

The display subsystem provides the logic to display a video frame from the memory frame buffer in either SDRAM on a liquid-crystal display (LCD) panel via the DVI-D interface. The DSS is configured in the 24 bit mode.

8.6.5 McBSP2

The multi-channel buffered serial port (McBSP) McBSP2 provides a full-duplex direct serial interface between the OMAP3 and the audio CODEC in the **TWL4030** using the I2S format. Only four signals are supported on the McBSP1 port. **Figure 28** is a depiction of McBSP2.

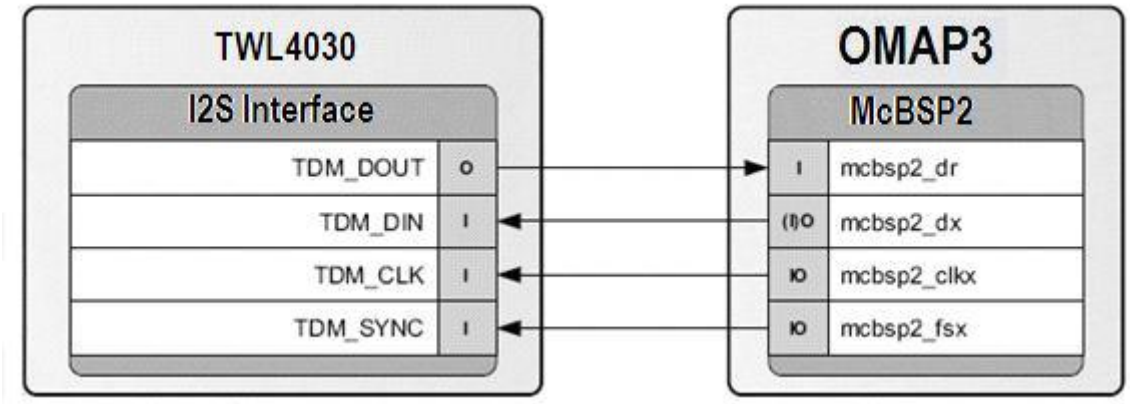

Figure 28. McBSP2 Interface

8.6.6 McBSP1

McBSP1 provides a full-duplex direct serial interface between the OMAP3 and the expansion interface. Only four signals are supported on McBSP1. **Figure 29** is a diagram of McBSP1.

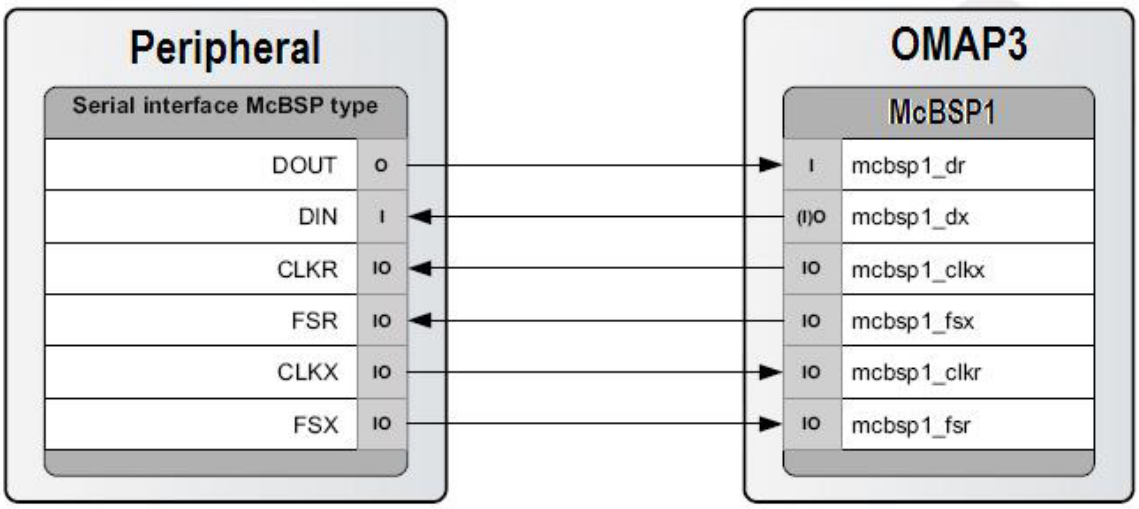

Figure 29. McBSP1 Interface

8.6.7 McBSP3

McBSP3 provides a full-duplex direct serial interface between the OMAP3 and the expansion interface. **Figure 30** is a diagram of McBSP3.

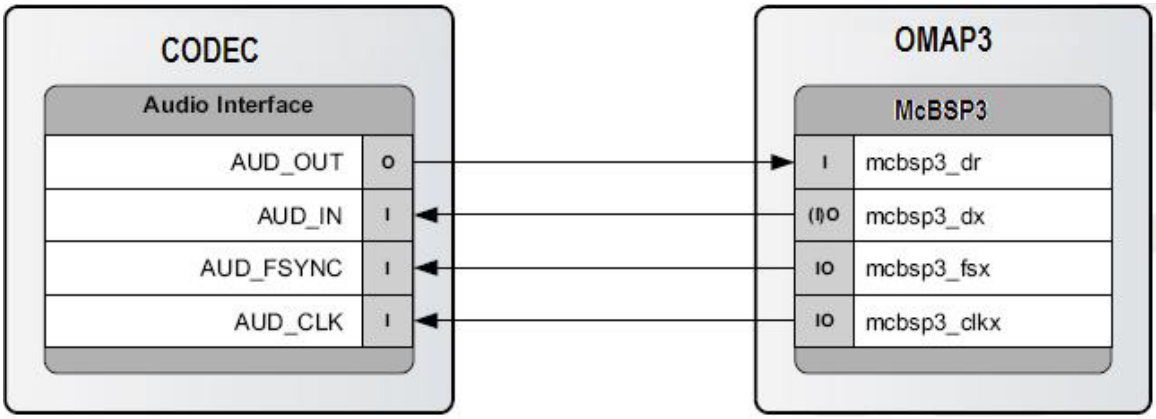

Figure 30. McBSP3 Interface

8.6.8 Pin Muxing

On the OMAP3, the majority of pins have multiple configurations that the pin can be set to. In essence, the pin can become different signals depending on how they are set in the software. In order for the Beagle to operate, the pins used must be set to the correct signal. In some cases, the default signal is the correct signal. Each pin can have a maximum of 7 options on the pin. This is called the pin mode and is indicated by a three bit values (0:3).

In the case of the signals going to the expansion connector, the settings required for those pins depends on how they are to be used. For an explanation of the options, please refer to the Expansion Header section.

Table 4 is a list of all of the signals used on the OMAP3 for the Beagle and the required mode setting for each pin. Where the default setting is needed, it will be indicated. The USER notation under mode indicates that this is an expansion signal and can be set at the discretion of the user. A FIXED indicates that there is only one function for that signal and that it cannot be changed,

Table 4. OMAP3 Pin Muxing Settings

Signal	Mode
DSS	Default
MMC1	Default
MMC2	User
UART3	Default
GPMC	Default
UART1	Default
I2C1	Default
I2C2	Default
I2C3	Default
I2C4	Default
JTAG	FIXED
TV_OUT	Default
SYS_nRESPWRON	Default
SYS_nRESWARM	Default
SYS_nIRQ	Default
SYS_OFF	Default
SYS_CLKOUT	Default
SYS_CLKOUT2	Default
SYS_CLKREQ	Default
SYS_XTALIN	FIXED
GPIO_149	4
GPIO_150	4
McBSP1	Default
McBSP2	User
McBSP3	Default

8.6.9 GPIO Mapping

There are a number of GPIO that are used on the Beagle design. **Table 5** shows which of these GPIO pins are used in the design and whether they are inputs or outputs. While GPIO pins can be used as interrupts, the table only covers the GPIO pin mode. If it is an interrupt, then it is covered in the interrupt section.

Table 5. OMAP3 GPIO Pins

OMAP PIN	INT/GPIO	I/O	Signal	USAGE
AA9	GPIO_149	O	LED_GPIO149	Controls User LED0
W8	GPIO_150	O	LED_GPIO149	Controls User LED1
AH8	GPIO_29	I	MMC1_WP	SD/MMC card slot Write protect
J25	GPIO_170	O	DVI_PUP	Controls the DVI-D interface. A Hi = DVI-D enabled.
AE7	GPIO_24	O	USBHS1_nCS	Enables/Disables the HS USB Host PHY
AE21	GPIO_7	I	SYSBOOT_5	Used to put the device in the boot mode or as a user button input

Other signals, such as those that connect to the expansion connector, may also be set as a GPIO pin. For information on those, refer to the Expansion Connector section.

8.6.10 Interrupt Mapping

There are a small number of pins on the OMAP3 that act as interrupt. Some of these interrupts are connected to the TWL4030 and their status is reflected through the main TWL4030 interrupt. **Table 6** lists the interrupts.

Table 6. OMAP3 Interrupt Pins

TWL4030 Pin	OMAP PIN	INT/GPIO	USAGE
	AF26	SYS_nIRQ	Interrupt from the TWL4030
	AH8	GPIO_29	SD Write protect lead. Can be polled or set to an interrupt.
P12		GPIO0	MMC1 card detect input. Goes to the OMAP3 over the SYS_nIRQ pin.
N12		GPIO1	USB Host over current detect input. Goes to the OMAP3 over the SYS_nIRQ pin.

8.7 POP Memory Device

The OMAP3 uses what is called POP (Package-on-Package) memory. The memory is a MCP (Multi Chip Package) that contains both the Mobile DDR SDRAM and the NAND Flash. **Figure 31** shows the POP Memory concept.

Figure 31. POP Memory

The Memory device mounts on top of the OMAP3 device. The configuration used on the board is a 2Gb NAND Flash plus 1Gb MDDR SDRAM device from Micron.

8.8 System Clocks

There are three clocks needed for the operation of the Beagle, 32KHz, 26MHz and McBSP_CLKS. **Figure 32** shows the components that make up the System Clocks.

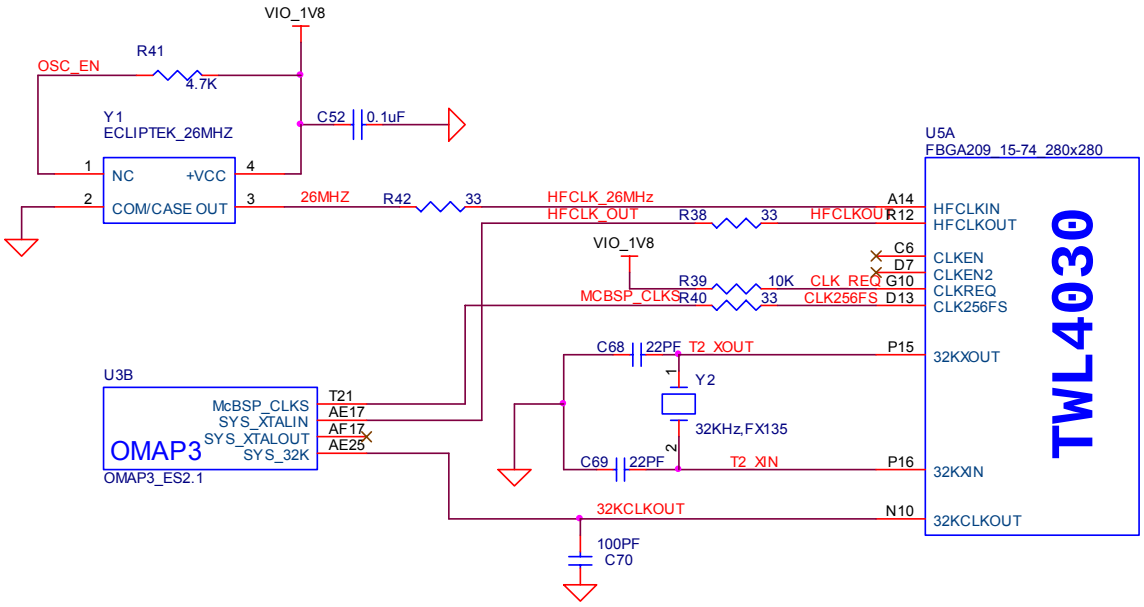

Figure 32. System Clocks

8.8.1 32KHz Clock

The 32KHz clock is needed for the T**WL4030** and the **OMAP3** and is provided by the **TWL4030** via the external 32KHz crystal, **Y2**. The **TWL4030** has a separate output from the crystal to drive the OMAP3 that buffers the resulting 32-kHz signal and provides it as **32KCLKOUT**, which is provided to the OMAP3 on ball **AE25**. The default mode of the 3**2KCLKOUT** signal is active, but it can be disabled if desired under SW control.

The 32.768-kHz clock drives the RTC embedded in the **TWL4030**. The RTC is not enabled by default; the host processor must set the correct date and time to enable the RTC.

8.8.2 26MHz Clock

This section describes the 26MHz clock section of the Beagle.

8.8.2.1 26MHz Source

The **26MHz** clock is provided by an onboard oscillator, **Y1**. The **TWL4030** receives the external **HFCLKIN** signal on ball **A14** and uses it to synchronize or generate the clocks required to operate the TWL4030 subsystems. The **TWL4030** must have this clock in order to function to the point where it can power up the Beagle. This is the reason the **26MHz** clock is routed through the TWL4030.

8.8.2.2 TWL4030 Setup

When the TWL4030 enters an active state, the OMAP3 must immediately indicate the **HFCLKIN** frequency (26 MHz) by setting the HFCLK_FREQ bit field (bits [1:0]) in the CFG_BOOT register of the TWL4030. HFCLK_FREQ has a default of not programmed, and in that condition, the USB subsection does not work, the three DCDC switching supplies (VIO, VDD1, and VDD2) operate from their free-running 3-MHz (RC) oscillators, and the PWR registers are accessed at a default 1.5-M byte. HFCLK_FREQ must be set by the OMAP3 during the initial power-up sequence. On Beagle, this is done by the internal boot ROM on startup.

8.8.2.3 OMAP3 26MHz

The 26MHz clock for the **OMAP3** is provided by the TWL4030 on ball **R12** through **R38**, a 33 ohm resistor is providing to minimize any reflections on the clock line. The clock signal enters via ball **AE17** on the **OMAP3**.

8.8.3 McBSP_CLKS

An additional clock is also provided by the **TWL40**30 called **McBSP_CL**KS. This clock is provided to the OMAP3 in order to insure synchronization of the I2S interface between the **OMAP3** and the **TWL4030**.

8.9 USB OTG Port

The main USB port on the Beagle is a USB OTG (On-the-Go) port. It can be used as an OTG port or Client port. The main use is as a client port, as that is the mode that will supply the power needed to power the Beagle.

***NOTE:* In order to use the OTG mode, the Beagle must be powered from the DC supply. Therefore, on Rev A5 boards, OTG is not supported.**

8.9.1 USB OTG Overview

USB OTG is a supplement to the USB 2.0 specification. The standard USB uses a master/slave architecture, a USB host acting as a master and a USB peripheral acting as a

slave. Only the USB host can schedule the configuration and data transfers over the link. The USB peripherals cannot initiate data transfers, they only respond to instructions given by a host.

USB OTG works differently in that gadgets don't need to be pure peripherals because they can sometimes act as hosts. An example might be connecting a USB keyboard or printer to Beagle or a USB printer that knows how to grab documents from certain peripherals and print them. The USB OTG compatible devices are able to initiate the session, control the connection and exchange Host/Peripheral roles between each other.

The USB OTG supplement does not prevent the use of a hub, but it describes role swapping only in the case of a one-to-one connection where two OTG devices are directly connected. If a standard hub is used, the supplement notes that using it will lead to losing USB OTG role-swap capabilities making one device as the Default-Host and the other as the Default-Peripheral until the hub is disconnected.

The combination of the OMAP3 and the TWL4030 allows the Beagle to work as an OTG device if desired. The primary mode of operation however, is intended to be a client mod in order to pull power from the USB host which is typically a PC.

8.9.2 USB OTG Design

Figure 33 is the design of the USB OTG port on the Beagle.

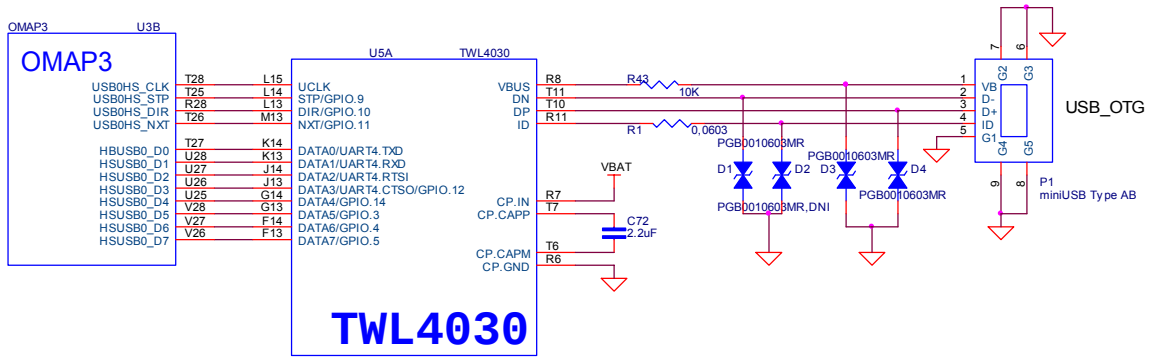

Figure 33. USB Client Design

8.9.3 OTG ULPI Interface

ULPI is an interface standard for high-speed USB 2.0 systems. It defines an interface between USB link controller (OMAP3) and the TWL4030 that drives the actual bus. ULPI stands for UTMI+ low pin interface and is designed specifically to reduce the pin count of discrete high-speed USB PHYs. Pin count reductions minimize the cost and footprint of the PHY chip on the PCB and reduce the number of pins dedicated to USB for the link controller.

.
Unlike full- and low-speed USB systems, which utilize serial interfaces, high-speed requires a parallel interface between the controller and PHY in order to run the bus at 480Mbps. This leads to a corresponding increase in complexity and pin count. The ULPI used on the Beagle keeps this down to only 12 signals because it combines just three control signals, plus clock, with a 8-bit bi-directional data bus. This bus is also used for the USB packet transmission and for accessing register data in the ULPI PHY.

8.9.3.1 OMAP3 Interface

The controller for the ULPI interface is the OMAP3. It provides all of the required signals to drive the interface. **Table 7** describes the signals form the OMAP3 that are used for the USB OTG interface.

Table 7. OMAP3 ULPI Interface

Signal	Description	Type	Ball
hsusb0_clk	Dedicated for external transceiver 60-MHz clock input from PHY	I	T28
hsusb0_stp	Dedicated for external transceiver Stop signal	O	T25
hsusb0_dir	Dedicated for external transceiver Data direction control from PHY	I	R28
hsusb0_nxt	Dedicated for external transceiver Next signal from PHY	I	T26
hsusb0_data0	Transceiver Bidirectional data bus	I/O	T27
hsusb0_data1	Transceiver Bidirectional data bus	I/O	U28
hsusb0_data2	Transceiver Bidirectional data bus	I/O	U27
hsusb0_data3	Transceiver Bidirectional data bus	I/O	U26
hsusb0_data4	Transceiver Bidirectional data bus	I/O	U25
hsusb0_data5	Transceiver Bidirectional data bus	I/O	V28
hsusb0_data6	Transceiver Bidirectional data bus	I/O	V27
hsusb0_data7	Transceiver Bidirectional data bus	I/O	V26

8.9.3.2 TWL4030 Interface

The TWL4030 USB interfaces to the OAMP3 over the ULPI interface. **Table 8** is a list of the signals used on the TWL4030 for the ULPI interface.

Table 8. OMAP3 ULPI Interface

Signal	Description	Type	Ball
UCLK	High speed USB clock	I/O	L15
STP	High speed USB stop	I	L14
DIR	High speed USB dir	O	L13
NXT	High speed USB direction	O	M1
DATA0	High speed USB Data bit 0	I/O	K14
DATA1	High speed USB Data bit 0	I/O	K13
DATA2	High speed USB Data bit 0	I/O	J14
DATA3	High speed USB Data bit 0	I/O	J13

DATA4	High speed USB Data bit 0	I/O	G14
DATA5	High speed USB Data bit 0	I/O	G13
DATA6	High speed USB Data bit 0	I/O	F14
DATA7	High speed USB Data bit 0	I/O	F13

8.9.4 OTG Charge Pump

When the TWL4030 acts as an A-device, the USB charge pump is used to provide 4.8 V/100 mA to the VBUS pin. When the TWL4030 acts as a B-device, the USB charge pump is in high impedance. If used in the OTG mode as an A-device, the Beagle will need to be powered from the DC supply. If acting as a B-device, there will not be a voltage source on the USB OTG port to drive the Beagle. **Table 9** describes the charge pump pins.

Table 9. USB OTG Charge Pump Pins

Signal	Description	Type	Ball
CP.IN	The charge pump input voltage. Connected to VBAT.	Power	R7
CP.CAPP	The charge pump flying capacitor plus.	O	L14
CP.CAPM	The charge pump flying capacitor minus.	O	T6
CP.GND	The charge pump ground.	GND	R6

The charge pump is powered by the **VBAT** voltage rail. The charge pump generates a 4.8-V (nominal) power supply voltage to the **VBUS** pin. The input voltage range is 2.7 V to 4.5 V so the 4.2V VBAT is within this range. The charge pump operating frequency is 1 MHz. The charge pump integrates a short-circuit current limitation at 450 mA.

8.9.5 OTG USB Connector

The OTG USB interface is accessed through a miniAB USB connector.

8.9.6 OTG USB Protection

Each lead on the USB port has ESD protection. IN order or the interface to meet the USB 2.0 Specification Eye Diagram, these protection devices must be low capacitance.

8.10 USB Host Port

A single High Speed USB Host port is provided to support USB based add on devices such as cameras, Hard Disk Drives, or other High Speed devices. Figure 34 is the circuitry that makes u the HS USB port.

Figure 33 is the design of the USB circuitry on the board.

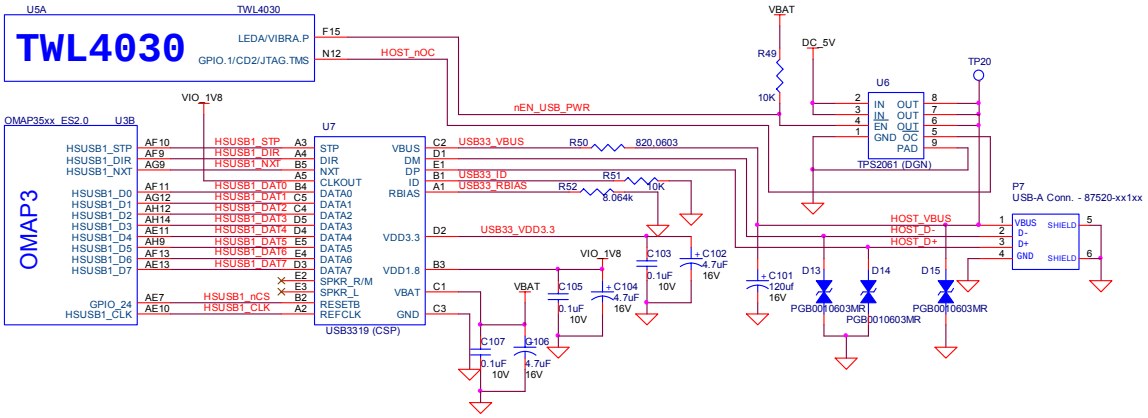

Figure 34. Host USB Port Design

NOTE: Beagle USB Host only supports HS USB (480Mbp/S). Low Speed and Full Speed devices are not supported unless they are connected through a USB Hub prior to connection to the Beagle. The OTG port does support LS and FS devices.

8.10.1 Host USB OMAP3 Interface

The interface to the OMAP3 is the HSUSB1 interface. The signals used on this interface are contained in **Table 10**.

Table 10. USB Host Port OMAP Signals

Signal	Description	Input/Output
hsusb1_clk	External transceiver 60-MHz clock output to PHY	O
hsusb1_stp	External transceiver Stop signal	O
hsusb1_dir	Transceiver data direction control from PHY	I
hsusb1_nxt	Next signal from PHY	I
hsusb1_data0	Bidirectional data bus signal for 12-pin ULPI operation	I/O
hsusb1_data1	Bidirectional data bus signal for 12-pin ULPI operation	I/O
hsusb1_data2	Bidirectional data bus signal for 12-pin ULPI operation	I/O
hsusb1_data3	Bidirectional data bus signal for 12-pin ULPI operation	I/O
hsusb1_data4	Bidirectional data bus signal for 12-pin ULPI operation	I/O
hsusb1_data5	Bidirectional data bus signal for 12-pin ULPI operation	I/O
hsusb1_data6	Bidirectional data bus signal for 12-pin ULPI operation	I/O
hsusb1_data7	Bidirectional data bus signal for 12-pin ULPI operation	I/O
Gpio_24	Enable/reset line to the USB PHY.	O

The **husb1_clk** signal is an output only and is used to support a HS USB PHY that supports an input clock mode. The SMSC PHY device supports this mode and is used on the Beagle.

8.10.2 Host USB PHY

The PHY used in the design is a USB3322 series device from SMSC. The USB33xx is a highly integrated Hi-Speed USB2.0 Transceiver (PHY) that meets all of the electrical requirements to be used as a Hi-Speed USB Host, Device, or an On-the-Go (OTG) transceiver. In this design, only the host mode of operation is being supported. The USB33xx uses the industry standard UTMI+ Low Pin Interface (ULPI) to connect the USB PHY to the OMAP3. ULPI uses a method of in-band signaling and status byte transfers between the Link and PHY to facilitate a USB session with only 12 pins.

In order to interface to the OMAP3, the device must be used in the 60MHz clock mode. This is done by tying the **CLKOUT** signal on the USB PHY to VIO_1V8. The clock for the PHY is derived from the 60MHz signal generated by the OMAP3. All of the signals and their functions align with the descriptions found in the OMAP3 Interface section.

The USB3322 device requires two voltages, the **VIO_1V8** rail to power the I/O rails and the **VBAT**, which needs to be between 3.1V and 5.1V, to power the rest of the device. On the board the **VBAT** is a regulated 4.2V DC. The 3.3V rail for the device is generated internally and requires a filter and bypass cap to be connected externally.

The **RBIAS** block in the PHY consists of an internal bandgap reference circuit used for generating the driver current and the biasing of the analog circuits. This block requires an external 8.06KΩ, 1% tolerance, reference resistor connected from **RBIAS** to ground. The nominal voltage at **RBIAS** is 0.8V and therefore the resistor will dissipate approximately 80µW of power.

The USB3322 can detect **ID** grounded and **ID** floating to determine if an A or B cable has been inserted. The A plug will ground the **ID** pin while the B plug will float the **ID** pin. As we are not using this device to support the OTG protocol but instead as a host device, we ground the **ID** pin to force it into a Host mode at all times. The **ID** signal is not present on the USB connector.

The USB33xx transceiver fully integrates all of the USB termination resistors on both **DP** and **DM**. This includes 1.5kΩ pull-up resistors, 15kΩ pull-down resistors and the 45Ω high speed termination resistors. These resistors require no tuning or trimming.

The ESD voltage suppressors, **D13**, **D14**, and **D15**, are intended to protect the USB circuits from ESD. These devices are especially suited for USB interfaces due to their low capacitance and low leakage current.

8.10.3 Host USB Connector

The USB connector used is a Type A receptacle. It provides connections for four signals, DP, DM, VBUS, and Ground. This is the same connector you will see on the back of a USB hub.

8.10.4 Host USB Power Control

Power is provided through the USB Host connector to power devices that are plugged in. This power can be controlled by the OMAP3 by controlling the **TPS2061** power switch.

The TPS2061 power-distribution switch is intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. This device incorporates a 70-mW N-channel MOSFET power switch. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The switch is controlled by the **TWL4030** using the **LED.A** signal. The OMAP3 uses the I2C interface to activate the signal in the TWL4030.

The amount of available current to be supplied depends on the remaining current available from the PC when in USB mode or the DC supply. The switch will not be able to supply more current than is available form the source.

The **TPS2061** also provides an overcurrent indicator and protection circuit. When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent (OC) logic output low. This is read by the **TWL4030** via the **CD2** pin. The **CD2** pin can be set to generate an interrupt to the OMAP3 to alert it of this condition.

When continuous heavy overloads and short-circuits increase the power dissipation in the switch, causing the junction temperature to rise, a thermal protection circuit shuts off the switch to prevent damage. Recovery from a thermal shutdown is automatic once the device has cooled sufficiently. Internal circuitry ensures that the switch remains off until valid input voltage is present. This power-distribution switch is designed to set current limit at 1.5 A typically. As mentioned, the amount of current available depends on the current source.

8.11 SD/MMC

The board provides and SD/MMC interface for using cards such as MMC memory cards and SDIO cards, such as cameras and Wireless LAN.

The connector supports 7 different types of cards.

- **SD-** Secure Digital (SD) is a flash memory card format developed by Matsushita, SanDisk and Toshiba for use in portable devices. As of 2007, SD card capacities range from 8 MB to 16 GB. Several companies have announced SD cards with 32 GB. Cards with 4-32 GB are considered high-capacity. The format has proven to be very popular. However, compatibility issues between older devices and the newer 4 GB and larger cards and the SDHC format have caused considerable confusion for some users. SD card have a write protect tab to prevent the data from being overwritten. SD supports 1-bit SD, 4-bit SD, and SPI modes.

- **miniSD-** Has the same features as the SD with the exceptions that it is in a smaller size and the support for 4-bit mode is optional amongst suppliers.

- **SDIO** - SDIO stands for Secure Digital Input Output. SD slots can actually be used for more than flash memory cards. Devices that support **SDIO** can use small devices designed for the SD form factor, like GPS receivers, Wi-Fi or Bluetooth adapters, modems, Ethernet adapters, barcode readers, IrDA adapters, FM radio tuners, TV tuners, RFID readers, digital cameras, or other mass storage media such as hard drives. SDIO cards are fully compatible with SD Memory Card host controller (including mechanical, electrical, power, signaling and software). When an SDIO card is inserted into a non SDIO-aware host, it will cause no physical damage or disruption to device or host controller. It should be noted that SPI bus topology is mandatory for SDIO, unlike SD Memory and most of the SD Memory commands are not supported in SDIO. **Figure 35** is an example of a SDIO camera card.

Figure 35. Example of an SDIO Card

- **MMC**- The Multi Media Card (**MMC**) is a flash memory card standard. Unveiled in 1997 by Siemens AG and SanDisk, it is based on Toshiba's NAND-based flash memory, and is therefore much smaller than earlier systems based on Intel NOR-based memory such as CompactFlash. MMC is about the size of a postage stamp: 24 mm x 32 mm x 1.4 mm. MMC originally used a 1-bit serial interface, but newer versions of the specification allow transfers of 4 at a time. MMCs are currently available in sizes up to and including 4 GB an 8 GB models.

- **MMCplus**- The version 4.x of the MMC standard, introduced in 2005, brought in two very significant changes to compete against SD cards. These were support for running at higher speeds (26MHz, 52MHz) than the original MMC (20MHz) or SD (25MHz, 50MHz). Version 4.x cards are fully backward compatible with existing readers but require updated hardware/software to use their new capabilities; even though the 4 bit wide bus and high-speed modes of operation are deliberately electrically compatible with SD, the initialization protocol is different, so firmware/software updates are required to allow these features to be enabled when the card is used in an SD reader.

- **MMCmobile** – Is basically the same as MMCplus except that it supports 8 bit data mode.

- **RS-MMC** –This alternate form factor is known as Reduced-Size MultiMediaCard, or RS-MMC, and was introduced in 2004. This form factor is a smaller form factor, of about half the size: 24 mm × 18 mm × 1.4 mm. RS-MMCs are simply smaller MMCs. RS-MMCs are currently available in sizes up to and including 4 GB. Nokia used to use RS-MMC in the Nokia 770 Internet Tablet. **Figure 35** is a side by side comparison of the RS-MMC and MMC card.

Figure 36. RS-MMC and Card

Figure 37 is the SD/MMC interface design on the Beagle.

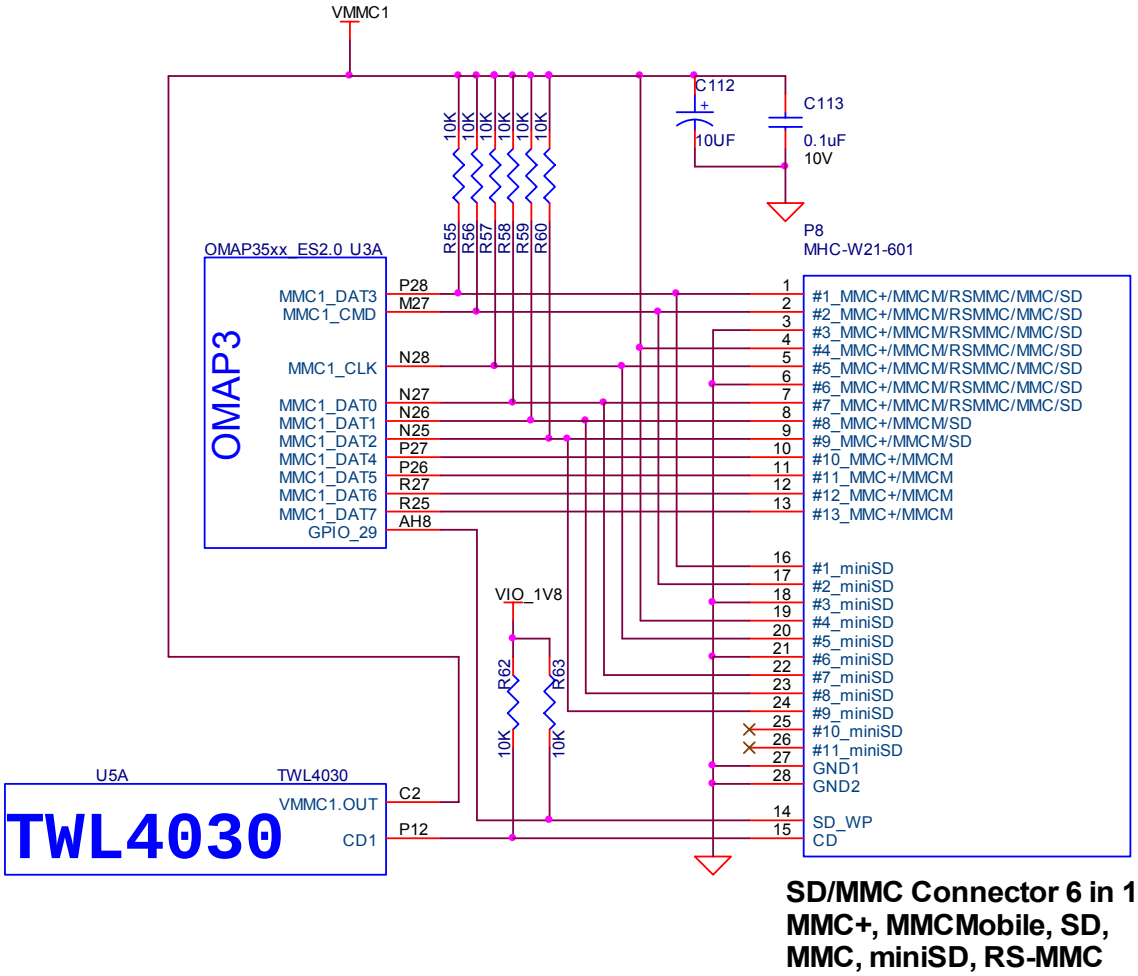

Figure 37. SD/MMC Interface

8.11.1 MMC Power

The SD/MMC connector is supplied power from the **TWL4030** using the **VMMC1** rail. The default setting on this rail is 3.0V as set by the Boot ROM and under SW control, can be set to 1.80V for use with 1.8V cards. The maximum current this rail can provide is 220mA as determined by the TWL4030 regulator. Maximum current can be limited bu the overall current available from the USB interface of the PC.

8.11.2 OMAP3 Interface

There are no external buffers required for the SD/MC operation. The OMAP3 provides all of the required interfaces for the SD/MMC interface.

The main features of the MMC/SD/SDIO host controller are:

- Full compliance with MMC command/response sets as defined in the *Multimedia Card System Specification*, v4.0
- Full compliance with SD command/response sets as defined in the *SD Memory Card Specifications*, v1.10d
- Full compliance with SDIO command/response sets and interrupt/read-wait mode as defined in the *SDIO Card Specification, Part E1*, v1.10
- Compliance with sets as defined in the *SD Card Specification, Part A2, SD Host Controller Standard Specification*, v1.00
- Full compliance with MMC bus testing procedure as defined in the *Multimedia Card System Specification*, v4.0
- Full compliance with CE-ATA command/response sets as defined in the *CE-ATA Standard Specification*
- Full compliance with ATA for MMCA specification
- Flexible architecture allowing support for new command structure
- Support:
  - 1-bit or 4-bit transfer mode specifications for SD and SDIO cards
  - 1-bit, 4-bit, or 8-bit transfer mode specifications for MMC cards
- Built-in 1024-byte buffer for read or write
- 32-bit-wide access bus to maximize bus throughput
- Single interrupt line for multiple interrupt source events
- Two slave DMA channels (1 for TX, 1 for RX)
- Programmable clock generation
- Support SDIO Read Wait and Suspend/Resume functions
- Support Stop at block gap
- Support command completion signal (CCS) and command completion signal disable (CCSD) management as specified in the *CE-ATA Standard Specification*

The known limitations are as follows:

- No built-in hardware support for error correction codes (ECC). See the *Multimedia Card System Specification*, v4.0, and the *SD Memory Card Specifications*, v1.10d, for details about ECC.
- The maximum block size defined in the *SD Memory Card Specifications*, v1.10d that the host driver can read and write to the buffer in the host controller is 2048 bytes. MMC supports a maximum block size of 1024 bytes. Up to 512 byte transfers, the buffer in MMC is considered as a double buffering with ping-pong management; half of the buffer can be written while the other part is read. For 512 to 1024 byte transfers, the entire buffer is dedicated to the transfer (read only or write only).

Table 11 provides a description of the signals on the MMC card.

Table 11. USB Host Port OMAP Signals

Signal Name	Description	I/O	Pin
MMC1_CLK	SD/MMC Clock output.	O	N28
MMC1_CMD	SD/MMC Command pin	I/O	M27
MMC1_DAT(0..7)	SD/MMC Data pins	I/O	N27,N26,N25,P28,P27, P26,R27,R25
MMC_WP	Write Protect detect	I	AH8

8.11.3 Card Detect

When a card is inserted into the SD/MMC connector, the Card Detect pin is grounded. This is detected on pin **P12** of the **TWL4030**. An interrupt, if enabled, is sent to the **OMAP3** via the interrupt pin. The SW can be written such that the system comes out of sleep or a reduced frequency mode when the card is detected.

8.11.4 Write Protect

If an SD card is inserted into the SD/MMC connector and the write protect pin is active, the Write Detect pin is grounded. This is detected **GPIO_29** of the OMAP3. The SW can then determine if the card is write protected and act accordingly.

8.11.5 8 Bit Mode

The Beagle also supports the new 8-bit cards. The upper 4 bits are supplied by the VDD_SIM power rail and as such the 8-bit mode is only supported in 1.8V modes. This requires that both the VMMC1 and VDD_SIM rails must be set to 1.8V when using 8 bit cards.

8.11.6 Booting From SD/MMC Cards

The ROM code supports booting from MMC and SD cards with some limitations:

- Support for MMC/SD cards compliant with the Multimedia Card System Specification v4.2 from the MMCA Technical Committee and the Secure Digital I/O Card Specification v2.0 from the SD Association. Including high-capacity (size >2GB) cards: HC-SD and HC MMC.
- 3-V power supply, 3-V I/O voltage on port 1
- Initial 1-bit MMC mode, 4-bit SD mode.
- Clock frequency:
  - Identification mode: 400 kHz
  - Data transfer mode: 20 MHz
- Only one card connected to the bus
- FAT12/16/32 support, with or without master boot sector (MBR).

The high-speed MMC/SD/SDIO host controllers handle the physical layer while the ROM code handles the simplified logical protocol layer (read-only protocol). A limited range of commands is implemented in the ROM code. The MMC/SD specification defines two operating voltages for standard or high-speed cards. The ROM code only supports standard operating voltage range (3-V) (both modes supported). The ROM code reads out a booting file from the card file system and boots from it.

8.12 Audio Interface

The Beagle supports stereo in and out through the **TWL4030** which provides the audio CODEC.

Figure 38 is the Audio circuitry design on the Beagle.

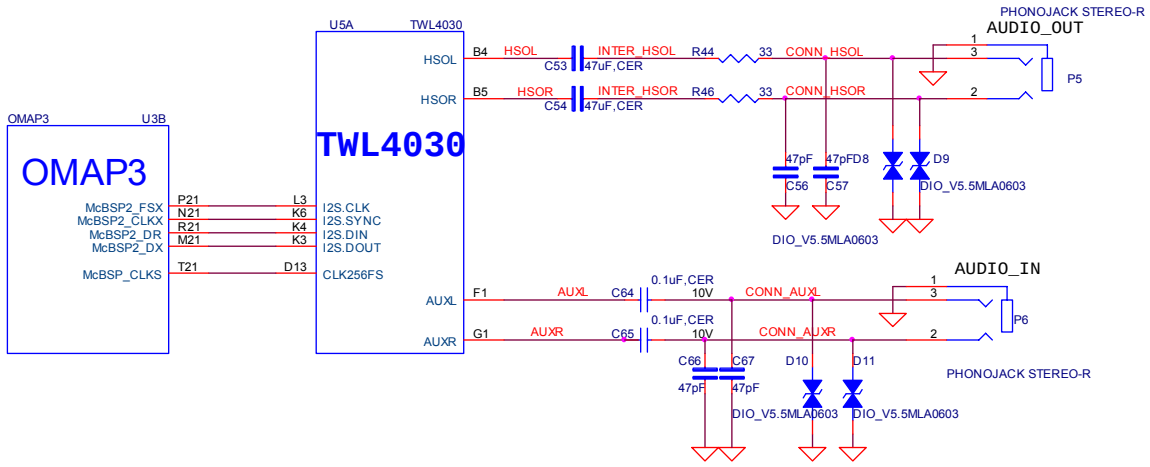

Figure 38. Audio Circuitry

8.12.1 OMAP3 Audio Interface

There are five McBSP modules called McBSP1 through McBSP5 on the OMAP3. **McBSP2** provides a full-duplex, direct serial interface between CODEC inside the TWL4030. It supports the I2S format to the TWL4030. In **Table 12** are the signals used on the OMAP3 to interface to the CODEC.

Table 12. OMAP3 Audio Signals

Signal Name	Description	I/O	Pin
mcbsp2_dr	Received serial data	I	R21
mcbsp2_dx	Transmitted serial data	I/O	M21
mcbsp2_clkx	Combined serial clock	I/O	N21
mcbsp2_fsx	Combined frame synchronization	I/O	P21
Mcbsp_clks	External clock input. Used to synchronize with the TWL4030	I	T21

8.12.2 TWL4030 Audio Interface

The **TWL4030** acts as a master or a slave for the I2S interface. If the **TWL4030** is the master, it must provide the frame synchronization (I2S_SYNC) and bit clock (I2S_CLK) to the **OMAP3**. If it is the slave, the **TWL4030** receives frame synchronization and bit clock. The TWL4030 supports the I2S, left-justified, and right-justified data formats, but doesn't support the TDM slave mode.

In **Table 13** are all the signals used to interface to the OMAP3.

Table 13. OMAP3 Audio Signals

Signal Name	Description	I/O	Pin
I2S.CLK	Clock signal (audio port)	I/O	L3
I2S.SYNC	Synchronization signal (audio port)	IO	K6
I2S.DIN	Data receive (audio port)	I	K4
I2S. DOUT	Data transmit (audio port)	O	K3
CLK256FS	Synchronization frame sync to the OMAP3	O	D13

8.12.3 Audio Output Jack

A single 3.5mm jack is provided on Beagle to support external stereo audio output devices such as headphones and powered speakers.

8.12.4 Audio Input Jack

A single 3.5mm jack is supplied to support external audio inputs including stereo or mono.

8.13 DVI Interface

The LCD interface on the **OMAP3** is accessible from the **DVI-D** interface connector on the board. **Figure 39** is the DVI-D design.

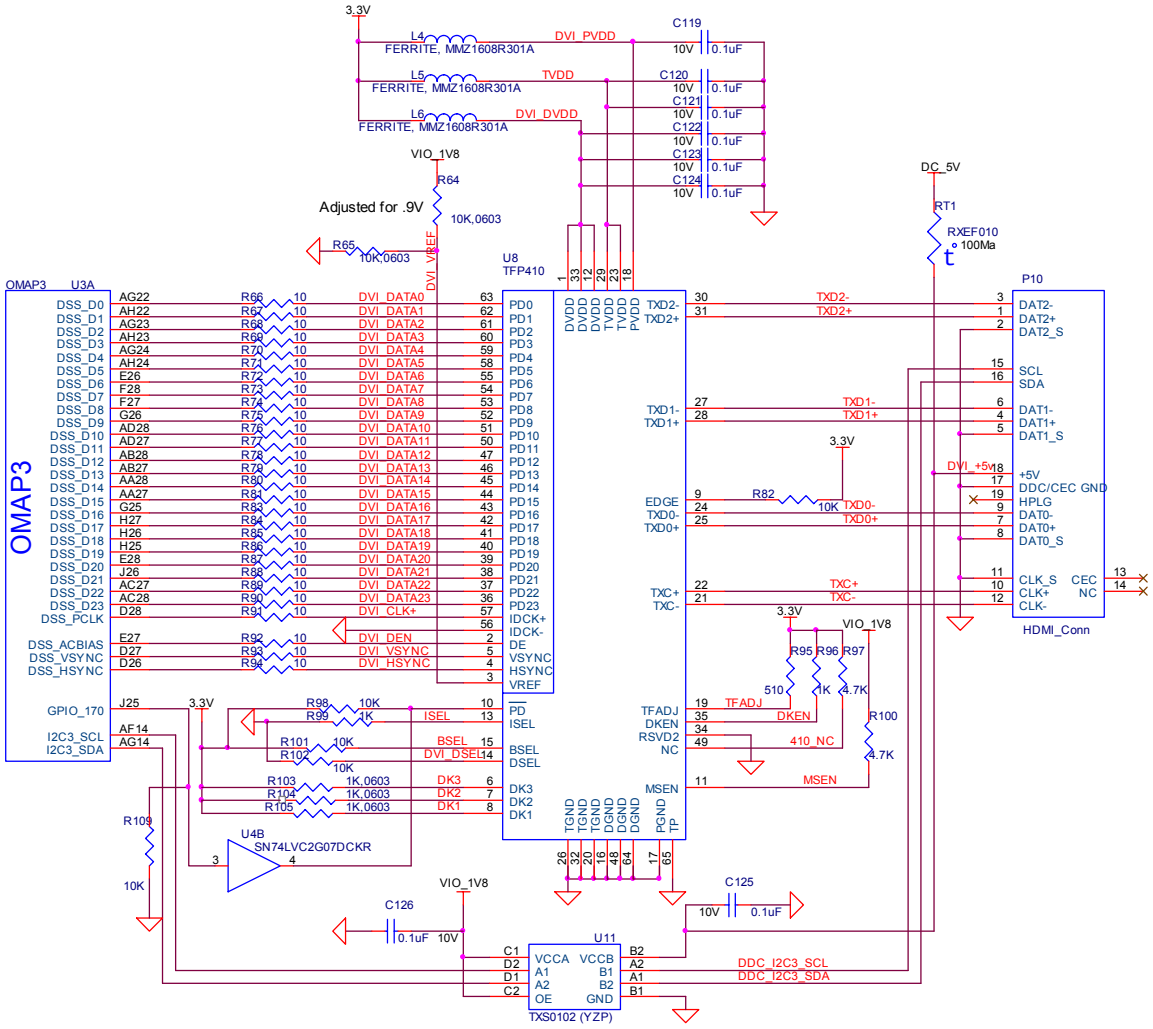

Figure 39. DVI-D Interface

8.13.1 OMAP3 LCD Interface

The main driver for the DVI-D interface originates at the **OMAP3** via the **DSS** pins. The OMAP3 provides 24 bits of data to the DVI-D framer chip, **TFP410**. There are three other signals used to control the DVI-D that originate at the **OMAP3**. These are I2C3_SCL, I2C3_SDA, and GPIO_170. All of the signals used are described in **Table 14.**

Table 14. OMAP3 LCD Signals

Signal Name	Description	Type	Ball
dss_pclk	LCD Pixel Clock	O	D28
dss_hsync	LCD Horizontal Synchronization	O	D26
dss_vsync	LCD Vertical Synchronization	O	D27
dss_acbias	Pixel data enable (TFT) output	O	E27
dss_data0	LCD Pixel Data bit 0	O	AG22
dss_data1	LCD Pixel Data bit 1	O	AH22
dss_data2	LCD Pixel Data bit 2	O	AG23
dss_data3	LCD Pixel Data bit 3	O	AH23
dss_data4	LCD Pixel Data bit 4	O	AG24
dss_data5	LCD Pixel Data bit 5	O	AH24
dss_data6	LCD Pixel Data bit 6	O	E26
dss_data7	LCD Pixel Data bit 7	O	F28
dss_data8	LCD Pixel Data bit 8	O	F27
dss_data9	LCD Pixel Data bit 9	O	G26
dss_data10	LCD Pixel Data bit 10	O	AD28
dss_data11	LCD Pixel Data bit 11	O	AD27
dss_data12	LCD Pixel Data bit 12	O	AB28
dss_data13	LCD Pixel Data bit 13	O	AB2
dss_data14	LCD Pixel Data bit 14	O	AA28
dss_data15	LCD Pixel Data bit 15	O	AA27
dss_data16 IO	LCD Pixel Data bit 16	O	G25
dss_data17	LCD Pixel Data bit 17	O	H27
dss_data18	LCD Pixel Data bit 18	O	H26
dss_data19	LCD Pixel Data bit 19	O	H25
dss_data20	LCD Pixel Data bit 20	O	E28
dss_data21	LCD Pixel Data bit 21	O	J26
dss_data22	LCD Pixel Data bit 22	O	AC27
dss_data23	LCD Pixel Data bit 23	O	AC28
GPIO_170	Powers down the TFP410 when Lo. TFP410 is active when Hi.	O	J25
I2C3_SCL	I2C3 clock line. Used to communicate with the monitor to determine setting information.	I/O	AF14
I2C3_SDA	I2C3 data line. Used to communicate with the monitor to determine setting information.	I/O	AG14

10ohm series resistors are provide in the signal path to minimize reflections in the high frequency signals from the **OMAP3** to the **TFP410**. These resistors are in the form of resistor packs on the Beagle. The maximum clock frequency of these signals is 65MHz.

8.13.2 OMAP3 LCD Power

In order for the DSS outputs to operate correctly out of the OMAP3, two voltage rails must be active, **VIO_1V8 and VDD_PLL2**. Both of these rails are controlled by the T**WL4030** and must be set to 1.8V. By default, **VDD_PLL2** is not turned and must be activated by SW. Otherwise some of the bits will not have power supplied to them.

8.13.3 TFP410 Framer

The **TFP410** provides a universal interface to allow a glue-less connection to provide the DVI-D digital interface to drive external LCD panels. The adjustable 1.1-V to 1.8-V digital interface provides a low-EMI, high-speed bus that connects seamlessly with the 1.8V and 24-bit interface output by the **OMAP3**. The DVI interface on the Beagle supports flat panel display resolutions up to XGA at 65 MHz in 24-bit true color pixel format.

Table 15 is a description of all of the interface and control pins on the **TFP410** and how they are used on Beagle.

Table 15. TFP410 Interface Signals

Signal Name	Description	Type	Ball
DATA[23:12]	The upper 12 bits of the 24-bit pixel bus.	I	36–47
DATA[11:0]	The bottom 12 bits of the 24-bit pixel bus.	I	50–55.56-53
IDCK+	Single ended clock input.	I	57
IDCK-	Tied to ground to support the single ended mode.	I	56
DE	Data enable. During active video (DE = high), the transmitter encodes pixel data, DATA[23:0]. During the blanking interval (DE = low), the transmitter encodes HSYNC and VSYNC.	I	2
HSYNC	Horizontal sync input	I	4
VSYNC	Vertical sync input	I	5
DK3	These three inputs are the de-skew inputs DK[3:1], used to adjust the setup and hold times of the pixel data inputs DATA[23:0], relative to the clock input IDCK±.	I	6
DK2		I	7
DK1		I	8
MSEN	A low level indicates a powered on receiver is detected at the differential outputs. A high level indicates a powered on receiver is not detected..	O	11
ISEL	This pin disables the I2C mode on chip. Configuration is specified by the configuration pins (BSEL, DSEL, EDGE, VREF) and state pins (PD, DKEN).	I	13
BSEL	Selects the 24bit and single-edge clock mode.	I	13
DSEL	Lo to select the single ended clock mode.	I	14
EDGE	A high level selects the primary latch to occur on the rising edge of the input clock IDCK	I	9
DKEN	A HI level enables the de-skew controlled by DK[1:3]	I	35
VREF	Sets the level of the input signals from the OMAP3.	I	3
PD	A HI selects normal operation and a LO selects the powerdown mode.	I	10
TGADJ	This pin controls the amplitude of the DVI output voltage swing, determined by the value of the pullup resistor RTFADJ connected to 3.3V.	I	19

8.13.4 TFP410 Power

Power to the TFP410 is supplied form the 3.3V regulator in **U1**, the **TPS2141**. In order to insure a noise free signal, there are three inductors, **L4**, **L5**, and **L6** that are used to filter the 3.3V rail into the TFP410.

8.13.5 TFP410 Control Pins

There are twelve control pins that set up the TFP410 to operate with the **OMAP3**. Most of these pins are set by HW and do not require any intervention by the **OMAP3** to set them.

8.13.5.1 ISEL

The **ISEL** pin is pulled LO via **R99** to place the TFP410 in the control pin mode with the I2C feature disabled. This allows the other modes for the TFP410 to be set by the other control pins.

8.13.5.2 BSEL

The **BSEL** pin is pulled HI to select the 24 bit mode for the Pixel Data interface from the OMAP3..

8.13.5.3 DSEL

The **DSEL** pin is pulled low to select the single ended clock mode from the **OMAP3**.

8.13.5.4 EDGE

The **EDGE** signal is pulled HI through **R82** to select the rising edge on the IDCK+ lead which is the pixel clock from the **OMAP3**.

8.13.5.5 DKEN

The **DKEN** signal is pulled HI to enable the de-skew pins. The de-skew pins, **DK1-DK3,** are pulled low by the internal pulldown resistors in the **TFP410**. This is the default mode of operation. If desired, the resistors can be installed to pull the signals high. However, it is not expected that any of the resistors will need to be installed. The DK1-DK3 pins adjust the timing of the clock as it relates to the data signals.

8.13.5.6 MSEN

The **MSEN** signal, when low, indicates that there is a powered monitor plugged into the DVI-D connector. This signal is not connected to the **OMAP3** and is provided as a test point only.

8.13.5.7 VREF

The **VREF** signal sets the voltage level of the **DATA**, **VSYNC**, **HSYNC**, **DE**, and **IDCK+** leads from the OMAP3. As the **OMAP3** is 1.8V, the level is set to .9V by **R64** and **R65**.

8.13.5.8 PD

The **PD** signal originates from the **OMAP3** on the GPIO_170 pin. Because the **P**D signal on the **TFP410** is 3.3V referenced, this signal must be converted to **3.3V**. This is done by **U4**, **SN74LVC2G07**, a non-inverting open drain buffer. If the **GPIO_170** pin is HI, then the open drain signal is inactive, causing the signal to be pulled HI by **R98**. When **GPIO_170** is taken low, the output of **U4** will also go LO, placing the **TFP410** in the power down mode. Even though **U4** is running at 1.8V to match the **OMAP3**, the output will support being pulled up to **3.3V**. On power up, the TFP410 is disabled by **R109**, a 10K resistor. When the **OMAP3** powers on, pin **J25** comes in a safe mode, meaning it is not being driven. R109 insures that the signal is pulled LO, putting the TFP410 in the power down mode.

8.13.5.9 TFADJ

The **TFADJ** signal controls the amplitude of the DVI output voltage swing, determined by the value of R95.

8.13.5.10 RSVD2

This unused pin is terminated to ground as directed by the TFP410 data manual.

8.13.5.11 NC

This unused pin is pulled HI as directed by the TFP410 data manual.

8.13.6 HDMI Connector

In order to minimize board size, a HDMI connector was selected for the DVI-D connection. The Beagle does not support HDMI but only the DVI-D component of HDMI. HDMI to DVI-D cables are available from numerous cable suppliers.

8.13.6.1 Shield Wire

Each signal has a shield wire that is used in the cable to provide signal protection for each differential pair. This signal is tied directly to ground.

8.13.6.2 DAT0+/DAT0-

The differential signal pair **DAT0+/DAT0-** transmits the 8-bit blue pixel data during active video and HSYNC and VSYNC during the blanking interval.

8.13.6.3 DAT1+/DAT1-

The differential signal pair **DAT1+/DAT1-** transmits the 8-bit green pixel data during active video.

8.13.6.4 DAT2+/DAT2-

The differential signal pair **DAT2+/DAT2-** transmits the 8-bit red pixel data during active.

8.13.6.5 TXC+/TXC-

The differential signal pair **TXC+/TXC-** transmits the differential clock from the TFP410.

8.13.6.6 DDC Channel

The **Display Data Channel** or **DDC (**sometimes referred to as EDID Enhanced Display ID**)** is a digital connection between a computer display and the **OMAP3** that allows the display specifications to be read by the **OMAP3**. The standard was created by the Video Electronics Standards Association (VESA). The current version of DDC, called DDC2B, is based on the I²C bus. The monitor contains a read-only memory (ROM) chip programmed by the manufacturer with information about the graphics modes that the monitor can display. This interface in the LCD panel is powered by the +5V pin on the connector through **RT1**, a resetable fuse. As the **OMAP**3 is 1.8V I/O, the I2C bus is level translated by **U11**, a **TXS0102**. It provides for a split rail to allow the signals to communicate. Inside of **TXS0102** is a pullup on each signal, removing the need for an external resistor.

8.14 S-Video

A single S-Video port is provided on the Beagle. **Figure 40** is the design of the S-Video interface.

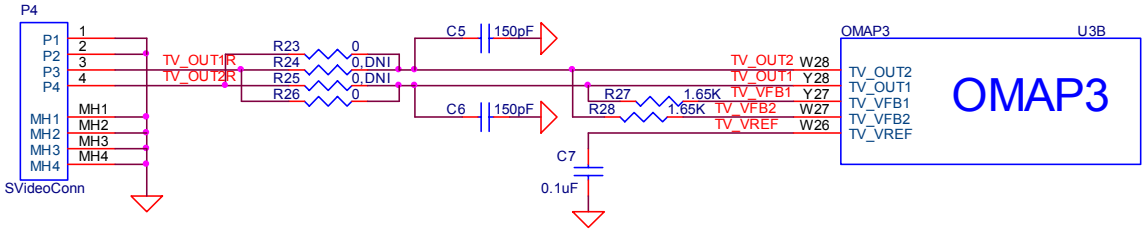

Figure 40. S-Video Interface

Table 16 is the list of the signals on the S-Video interface and their definitions.

Table 16. TFP410 Interface Signals

Signal	I/O	Description
tv_out1	O	TV analog output composite
tv_out2	O	TV analog output S-VIDEO
tv_vref	I	Reference output voltage from internal bandgap
tv_vfb1	O	Amplifier feedback node
tv_vfb2	O	Amplifier feedback node

You will notice a bank of four resistors, **R23**, **R24**, **R25**, and **R26**, on the S-Video output. In the earlier ES2.0 version of the **OMAP3** the **TV_OUT1** (Luminance) and TV_OUT2 (Chrominance) signals were swapped. In order to support both revisions of the silicon, the Beagle was designed with resistors to allow for the configuring of the **OMAP3** for the silicon version used. The default configuration will be to load **R23** and **R26** to allow the signals to go straight through. Notice that the signal names are in a different order than they are on the **OMAP3**. So, while it appears that the resistors loaded create a swap in the signals, in reality they do not.

8.15 RS232 Port

A single RS232 port is provided on the Beagle. It provides access to the TX and RX lines of **UART3** on the OMAP3. **Figure 41** shows the design of the RS232 port.

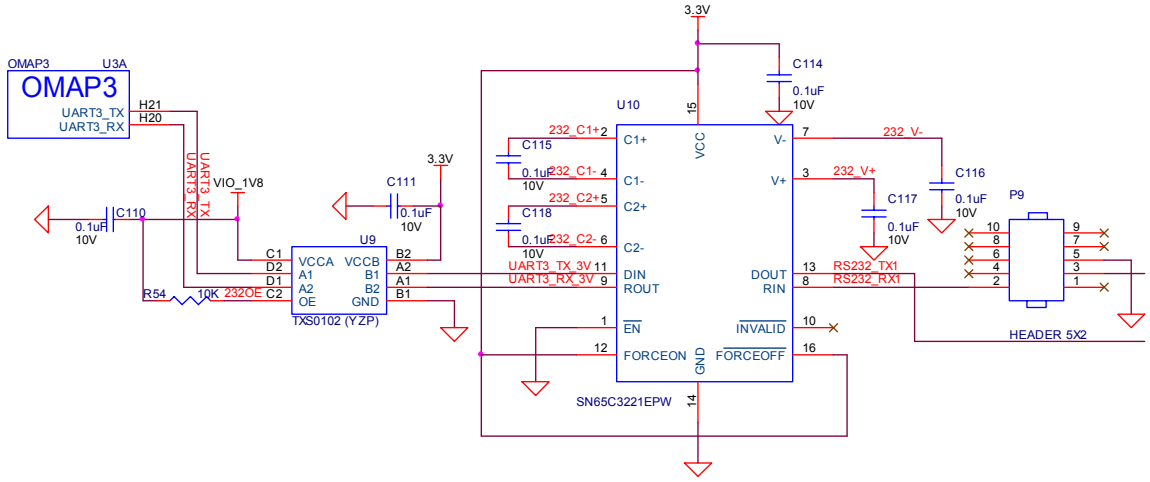

Figure 41. RS232 Interface Design

8.15.1 OMAP3 Interface

Two lines, **UART3_Tx** and **UART3_Rx**, are provided by the OMAP3. The **UART3** function contains a programmable baud generator and a set of fixed dividers that divide the 48-MHz clock input down to the expected baud rate and also supports auto bauding.

8.15.2 OMAP3 Level Translator

All of the I/O levels from the OMAP3 are **1.8V** while the transceiver used runs at 3.3V. This requires that the voltage levels be translated. This is accomplished by the TXS0102 which is a two-bit noninverting translator that uses two separate configurable power-supply rails. The A port tracks VCCA, 1.8V and the B port tracks VCCB, 3.3V. This allows for low-voltage bidirectional translation between the two voltage nodes. When the output-enable (OE) input is low, all outputs are placed in the high-impedance state. In this design, the OE is tied high via a 10K ohm resistor to insure that it is always on.

8.15.3 RS232 Transceiver

The RS232 transceiver used is the SN65C3221. The SN65C3221 consist of one line driver, one line receiver, and a dual charge-pump circuit with ±15-kV IEC ESD protection pin to pin (serial-port connection pins, including GND). These devices provide the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from

a single 3-V to 5.5-V supply. The **SN65C3221** operates at data signaling rates up to 1 Mbit/s and a driver output slew rate of 24 V/ms to 150 V/ms. While the **OMAP3** can easily drive a 1Mbit/S rate, your results may vary based on cabling, distance, and the loads and drive capability on the other end of the RS232 port.

The transceiver is powered from the 3.3V rail and is active at power up. This allows the port to be used for UART based peripheral booting over the port.

8.15.4 Connector

Access to the RS232 port is through a 10pin header, **P9**. Connection to the header is through a 10 pin IDC to 9 pin D-sub cable. This header requires the use of an ATI-Everex type cable. This is the only cable that will work. This cable is readily available from a number of sources and is commonly found on many PC motherboards. **Figure 41** is a picture of what the cable assembly looks like.

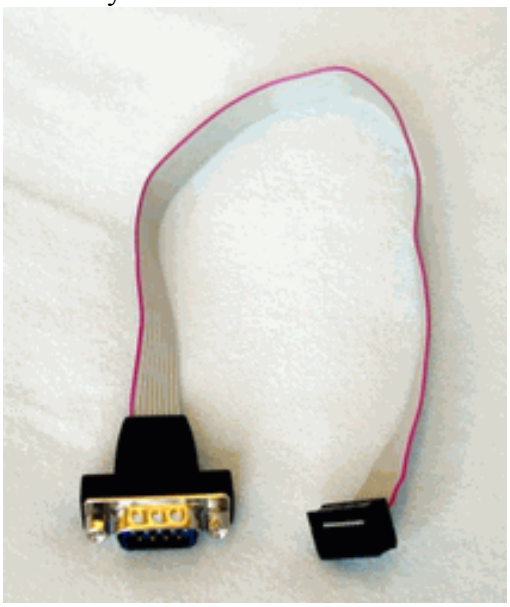

Figure 42. RS232 Cable

When purchasing, make sure the ATI-Everex or pass through cable is ordered.

8.16 Indicators

There are four green indicators on the Beagle:

- Power
- PMU_STAT
- USER0
- USER1

Three of these are programmable under SW control and the fourth one is tied to the main power rail.

Figure 43 shows the connection of all of these indicators.

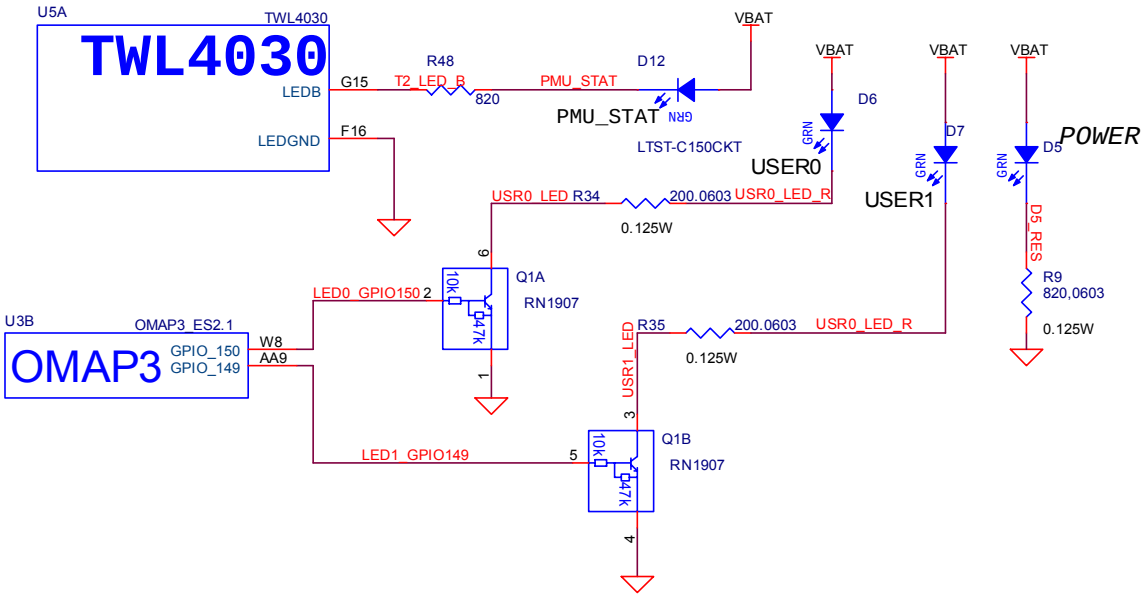

Figure 43. Indicator Design

8.16.1 Power Indicator

This indicator, **D7**, connects across the **VBAT** supply and ground. It indicates that the entire power path is supplying the power to the board. The **VBAT** regulator can be driven from either the USB Client port or an external 5VDC power supply. Indicator **D7** does not indicate where one or the other is being used to supply the main power to the board.

8.16.2 PMU Status Indicator

This output is driven from the **TWL4030** using the **LED.B** output. The **TWL4030** provides LED driver circuitry to power two LED circuits that can provide user indicators. The first circuit can provide up to 160 mA and the second, 50 mA. Each LED circuit is independently controllable for basic power (on/off) control and illumination level (using PWM). The second driver, **LED.B**, is used to drive an LED that is connected to the VBAT rail through a resistor.

The PWM inside the TWL4030 can be used to alter the brightness of the LED if desired or it can be turned on or off by the **OMAP3** using the I2C bus. The PWM is programmable, register-controlled, duty cycle based on a nominal 4-Hz cycle which is derived from an internal 32-kHz clock. It is possible to set the LED to flash automatically without SW control if desired.

8.16.3 User Indicators

There are two user LEDs that can be driven directly from a GPIO pin on the **OMAP3**. These can be used for any purpose by the SW. The output level of the **OMAP3** is 1.8V and the current sink capability is not enough to drive an LED with any level of brightness. A transistor pair, **RN1907** is used to drive the LEDs from the **VBAT** rail. A logic level of 1 will turn the LED on.

8.17 JTAG

A JTAG header is provided to allow for advanced debugging on the Beagle Board by using a JTAG based debugger **Figure 44** shows the interconnection to the OMAP3 processor.

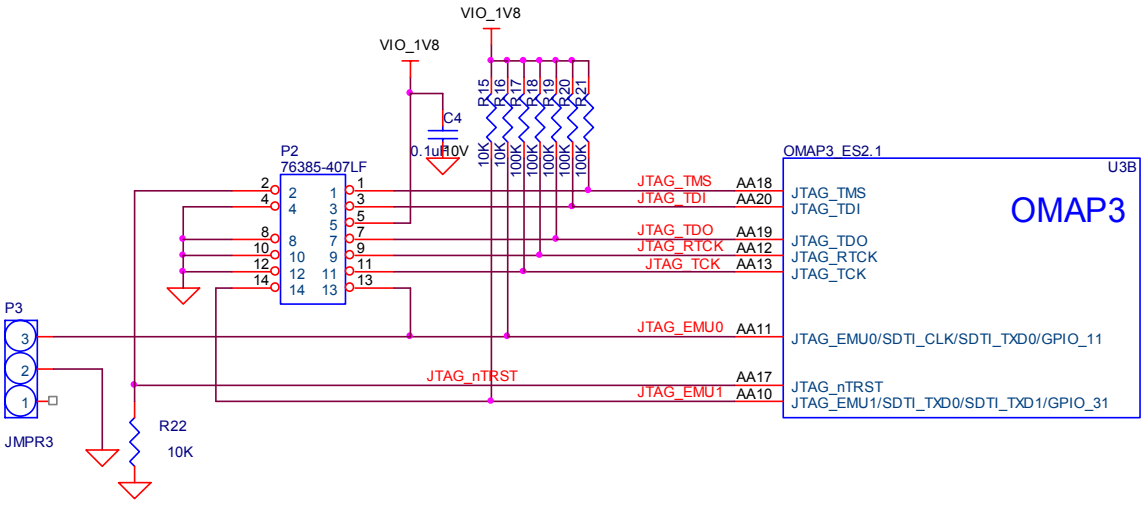

Figure 44. JTAG Interface

8.17.1 OMAP3 Interface

The JTAG interface connects directly to the OMAP processor. All signals are a 1.8V level. **Table 17** describes the signals on the JTAG connector.

Table 17. JTAG Signals

Signal	Description	I/O
JTAG_TMS	Test mode select	I/O
JTAG_TDI	Test data input	I
JTAG_TDO	Test Data Output	O
JTAG_RTCK	ARM Clock Emulation	O
JTAG_TCK	Test Clock	I
JTAG_nTRST	Test reset	I
JTAG_EMU0	Test emulation 0	I/O
JTAG_EMU1	Test emulation 1	I/O

8.17.2 Connector

The JTAG interface uses a 14 pin connector. All JTAG emulator modules should be able to support this interface. Contact your emulator supplier for further information or if an adapter is needed.

8.17.3 Optional P3 Jumper

There is an optional jumper on the board labeled **J3**. This is required on some versions of the **OMAP3** processor to insure that the JTAG will be able to connect. On the ES2.1 version of the **OMAP3** used for the Beagle the jumper is not needed and is therefore not populated. If needed, the jumper can be installed.

8.18 Expansion Header

The expansion header is provided to allow a limited number of functions to be added to the board via the addition of a daughtercard.

Figure 45 is the design of the expansion connector and the interfaces to the OMAP3.

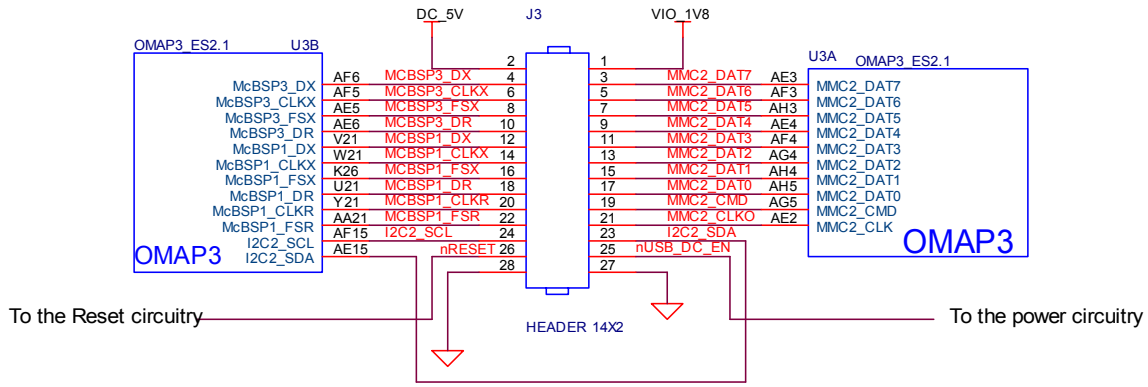

Figure 45. Expansion Header

8.18.1 OMAP3 Interface

The main purpose of the expansion connector is to route additional signals from the **OMAP3** processor. **Table 18** shows all of the signals that are on the expansion header. As the **OMAP3** has a multiplexing feature, multiple signals can be connected to certain pins to add additional options as it pertains to the signal available. The different columns in **Table 18** show what other signals can be accessed by setting the mux control register in the **OMAP3**.

It should be noted that there are additional signals available on some of these pins. These were left off of the table as they have no real value due to the set of signals being incomplete to implement certain functions.

The expansion signals are explained further in the next section.

Table 18. Expansion Connector Signals

Pin	Option A	Option B	Option C	Option D
1	VIO_1V8			
2	DC_5V			
3	MMC2_DAT7	GPIO_139		
4	McBSP3_DX	GPIO_140	UART2_CTS	
5	MMC2_DAT6	GPIO_138		
6	McBSP3_CLKX	GPIO_141	UART2_RTS	
7	MMC2_DAT5	GPIO_137		
8	McBSP3_FSX	GPIO_143	UART2_RX	
9	MMC2_DAT4	GPIO_136		
10	McBSP3_DR	GPIO_142	UART2_TX	
11	MMC2_DAT3	McSPI3_CS0	GPIO_135	
12	McBSP1_DX	McSPI4_SIMO	McBSP3_DX	GPIO_158
13	MMC2_DAT2	McSPI3_CS1	GPIO_134	
14	McBSP1_CLKX	McBSP3_CLKX	GPIO_162	
15	MMC2_DAT1	GPIO_133		
16	McBSP1_FSX	McSPI4_CS0	McBSP3_FSX	GPIO_161
17	MMC2_DAT0	McSPI3_SOMI	GPIO_132	
18	McBSP1_DR	McSPI4_SOMI	McBSP3_DR	GPIO_159
19	MMC2_CMD	McSPI3_SIMO	GPIO_131	
20	McBSP1_CLKR	McSPI4_CLK	SIM_CD	GPIO_156
21	MMC2_CLKO	McSPI3_CLK	GPIO_130	
22	McBSP1_FSR			GPIO_157
23	I2C2_SDA	GPIO_183		
24	I2C2_SCL	GPIO_168		
25	REGEN			
26	nRESET			
27	GND			
28	GND			

8.18.2 Expansion Signals

This section provides more detail on each of the signals available on the expansion connector. They are grouped by functions in **Table 19** along with a description of each signal.

If you use these signals in their respective groups and that is the only function you use, all of the signals are available. Whether or not the signals you need are all available, depends on the muxing function on a per pin bases. Only one signal per pin is available at any one time.

Table 19. Expansion Connector Signals

Signal	Description	I/O	Pin
SD/MMC Port 2			
MMC2_DAT7	SD/MMC data pin 7.		
MMC2_DAT6	SD/MMC data pin 6.		
MMC2_DAT5	SD/MMC data pin 5.		
MMC2_DAT4	SD/MMC data pin 4.		
MMC2_DAT3	SD/MMC data pin 3.		
MMC2_DAT2	SD/MMC data pin 2.		
MMC2_DAT1	SD/MMC data pin 1.		
MMC2_DAT0	SD/MMC data pin 0.		
MMC2_CMD	SD/MMC command signal.		
MMC_CLKO	SD/MMC clock signal.		
McBSP1 Port 2			
McBSP1_DX	Multi channel buffered serial port transmit		
McBSP1_CLKX	Multi channel buffered serial port transmit clock		
McBSP1_FSX	Multi channel buffered serial port transmit frame sync		
McBSP1_DR	Multi channel buffered serial port receive		
McBSP1_CLKR	Multi channel buffered serial port receive clock		
I2C Port 2			
I2C2_SDA	I2C data line.		
I2C2_SCL	I2C clock line		
McBSP Port 3			
McBSP3_DR	Multi channel buffered serial port receive		
McBSP3_DX	Multi channel buffered serial port transmit		
McBSP3_CLKX	Multi channel buffered serial port receive clock		
McBSP3_FSX	Multi channel buffered serial port frame sync transmit		
General Purpose I/O Pins			
GPIO_130	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_131	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_132	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_133	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_134	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_135	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_136	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_137	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_138	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_139	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_140	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_141	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_142	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_143	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_156	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_157	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_158	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_161	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_162	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_168	General Purpose Input/Output pin. Can be used as an interrupt pin.		
GPIO_183	General Purpose Input/Output pin. Can be used as an interrupt pin.		
McSPI Port 3			
McSPI3_CS0	Multi channel SPI chip select 0		
McSPI3_CS1	Multi channel SPI chip select 1		
McSPI3_SIMO	Multi channel SPI slave in master out		
McSPI3_SOMI	Multi channel SPI slave out master in		
McSPI3_CLK	Multi channel SPI clock		
McSPI Port 4			
McSPI4_SIMO	Multi channel SPI slave in master out		
McSPI4_SOMI	Multi channel SPI slave out master in		
McSPI4_CS0	Multi channel SPI chip select 0		
McSPI4_CLK	Multi channel SPI clock		
UART Port 2			
UART2_CTS	UART clear to send.		
UART2_RTS	UART request to send		
UART2_RX	UART receive		
UART2_TX	UART transmit		

8.18.3 Power

The expansion connector provides two power rails. The first is the **VIO_1.8V** rail which is supplied by the **TWL4030**. This rail is limited in the current it can supply from the **TWL4030** and what remains from the current consumed by the Beagle and is intended to be used to provide a rail for voltage level conversion. It is not intended to power a lot of circuitry on the expansion board. All signals from the Beagle are at 1.8V.

The other rail is the **DC_5V**. The same restriction exits on this rail as mentioned in the USB section. The amount of available power to an expansion board depends on the available power from the DC supply or the USB supply from the PC.

8.18.4 Reset

The **nRESET** signal is the main board reset signal. When the board powers up, this signal will act as an input to reset circuitry on the expansion board. After power up, a system reset can be generated by the expansion board by taking this signal low. This signal is a 1.8V level signal.

8.18.5 Power Control

There is an additional open-drain signal on the connector called **REGEN**. The purpose of this signal is to provide a means to control power circuitry on the expansion card to turn on and off the voltages. This insures that the power on the board is turned on at the appropriate time. Depending on what circuitry is provided on the expansion card, an additional delay may be needed to be added before the circuitry is activated. Refer to the **OMAP3** and **TWL4030** documentation for more information.

9.0 Connector Pinouts and Cables

This section provides a definition of the pinouts and cables to be used with all of the connectors and headers on the Beagle.

9.1 Power

Figure 46 is a picture of the Beagle power connector with the pins identified.

To Be Added on Rev B.

Figure 46. Power Connector

NOTE: Revision A5 boards do not have power connectors on them.

9.2 USB OTG

Figure 47 is a picture of the Beagle USB OTG connector with the pins identified.

To Be Added on Next Revision.

Figure 47. USB OTG Connector

9.3 USB Host

Figure 48 is a picture of the Beagle USB OTG connector with the pins identified.

To Be Added on Next Revision.

Figure 48. USB Host Connector

9.4 S-Video

Figure 49 is the S-Video connector on the Beagle.

To Be Added on Next Revision.

Figure 49. S-Video Connector

9.5 DVI-D

Figure 50 is the pinout of the HDMI connector on Beagle.

To Be Added on Next Revision.

Figure 50. HDMI Connector

Figure 51 is the HDMI to DVI-D connector used to connect to an LCD monitor.

To Be Added

Figure 51. HDMI to DVI-D Cable

9.6 Audio In

Figure 52 is the Audio In connector.

To Be Added on Next Revision.

Figure 52. Audio Out Connector

9.7 Audio Out

Figure 53 is the audio out connector.

To Be Added on Next Revision.

Figure 53. Audio Out Connector

9.8 JTAG

Figure 54 is the JTAG connector pin out.

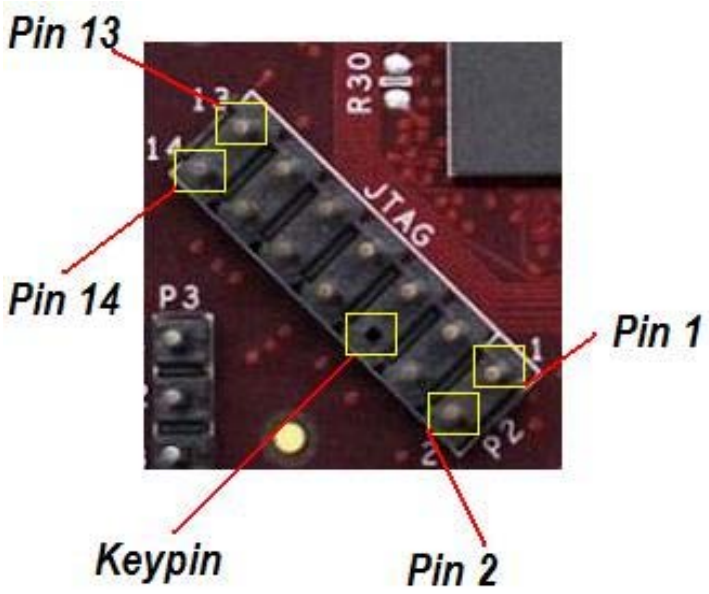

Figure 54. JTAG Connector Pinout

Table 20 gives a definition of each of the signals on the JTAG header.

Table 20. JTAG Signals

Signal	Description	I/O
JTAG_TMS	Test mode select	I/O
JTAG_TDI	Test data input	I
JTAG_TDO	Test Data Output	O
JTAG_RTCK	ARM Clock Emulation	O
JTAG_TCK	Test Clock	I
JTAG_nTRST	Test reset	I
JTAG_EMU0	Test emulation 0	I/O
JTAG_EMU1	Test emulation 1	I/O

9.9 RS232

Figure 55 is the RS232 header on the Beagle with the pin numbers identified.

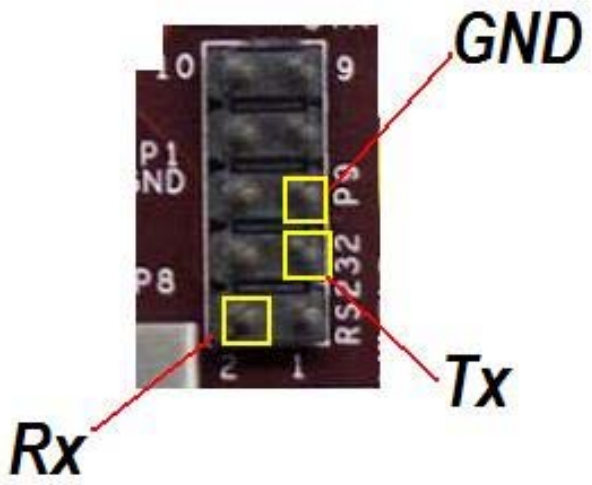

Figure 55. RS232 Header

Figure 56 is the cable that is required in order to access the RS232 header. This cable can be purchased from various sources and is referred to as the ATI/Everex type cable.

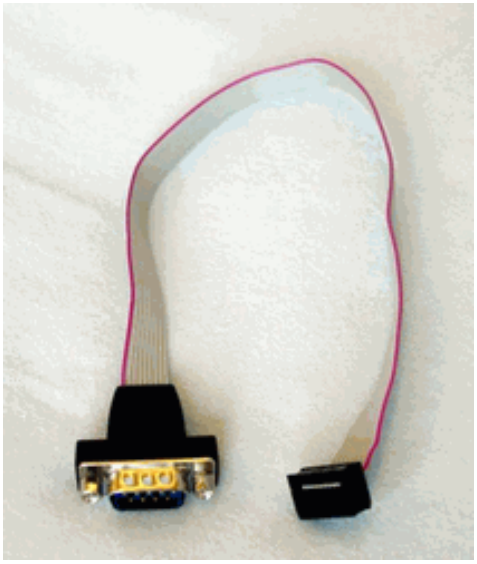

Figure 56. RS232 Flat Cable

9.10 Expansion

Figure 57 is the pinout of the expansion header on the Beagle.

Figure 57. Expansion Header

Table 21 is the signals on the Expansion Connector.

Table 21. Expansion Connector Signals

Pin	Option A	Option B	Option C	Option D
1	VIO_1V8			
2	DC_5V			
3	MMC2_DAT7	GPIO_139		
4	McBSP3_DX	GPIO_140	UART2_CTS	
5	MMC2_DAT6	GPIO_138		
6	McBSP3_CLKX	GPIO_141	UART2_RTS	
7	MMC2_DAT5	GPIO_137		
8	McBSP3_FSX	GPIO_143	UART2_RX	
9	MMC2_DAT4	GPIO_136		
10	McBSP3_DR	GPIO_142	UART2_TX	
11	MMC2_DAT3	McSPI3_CS0	GPIO_135	
12	McBSP1_DX	McSPI4_SIMO	McBSP3_DX	GPIO_158
13	MMC2_DAT2	McSPI3_CS1	GPIO_134	
14	McBSP1_CLKX	McBSP3_CLKX	GPIO_162	
15	MMC2_DAT1	GPIO_133		
16	McBSP1_FSX	McSPI4_CS0	McBSP3_FSX	GPIO_161
17	MMC2_DAT0	McSPI3_SOMI	GPIO_132	
18	McBSP1_DR	McSPI4_SOMI	McBSP3_DR	GPIO_159
19	MMC2_CMD	McSPI3_SIMO	GPIO_131	
20	McBSP1_CLKR	McSPI4_CLK	SIM_CD	GPIO_156
21	MMC2_CLKO	McSPI3_CLK	GPIO_130	
22	McBSP1_FSR			
23	I2C2_SDA	GPIO_183		
24	I2C2_SCL	GPIO_168		
25	REGEN			
26	nRESET			
27	GND			
28	GND			

10.0 Beagle Accessories

Throughout this manual various items are mentioned as not being provided with the standard Beagle package or as options to extend the features of the Beagle. The concept behind Beagle is that different features and functions can be added to Beagle by bringing your own peripherals. This has several key advantages:

- User can choose which peripherals to add.
- User can choose the brand of peripherals based on driver availability and ability to acquire the particular peripheral
- User can add these peripherals at a lower cost than if they were integrated into the Beagle.

This section covers these accessories and add-ons and provides information on where they may be obtained. Obviously things can change very quickly as it relates to devices that may be available. Please check beagleboard.org for an up to date listing of these peripherals.

Inclusion of any products in this section does not guarantee that they will operate with all SW releases. It is up to the user to find the appropriate drivers for each of these products. Information provided here is intended to expose the capabilities of what can be done with the Beagle and how it can be expanded.

All pricing information provided is subject to change an din most cases is likely to be lower depending on the products purchased and from where they are purchased.

Covered in this section are the following accessories:

- DC Power Supplies
- Serial Ribbon cable
- USB Hubs
- USB Thumb Drives
- DVI-D to HDMI Cables
- DVI-D Monitors
- SD/MMC Cards
- USB to Ethernet
- USB to WiFi
- USB Bluetooth
- Expansion Cards

10.1 DC Power Supply

Tabletop or wall plug supplies can be used to power Beagle. **Table 22** provides the specifications for the Beagle DC supply. Supplies that provide additional current than what is specified can be used if additional current is needed for add on accessories. The amount specified is equal to that supplied by a USB port.

Table 22. DC Power Supply Specifications

Specification	Requirement	Unit
Voltage	5.0	V
Current	500mA (minimum)	mA
Connector	2.1mm x 5.5mm Center hot	

It is recommended that a supply higher than 500mA be used if higher current peripherals are expected to be used or if expansion boards are added.

Table 23 lists some power supplies that will work with the beagle.

Table 23. DC Power Supplies

Part #	Manufacturer	Supplier	Price
DCU090050E2961	RELIAPRO	Jameco	$4.99

Figure 58 is a picture of the type of power supply that will be used on the Beagle.

Figure 58. DC Power Supply

10.2 Serial Ribbon Cable

Figure 59 is the serial ribbon cable for the Beagle.

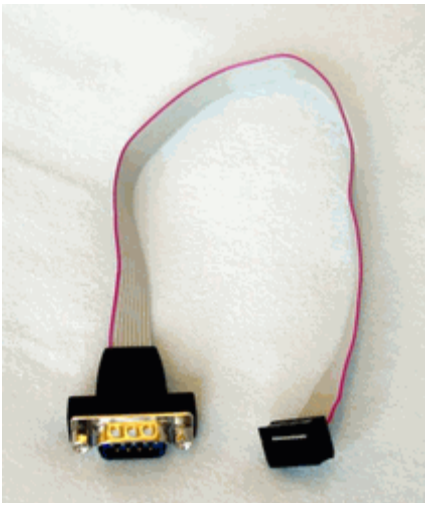

Figure 59. RS232 Cable

If you like, you can also make your own cable. **Figure 59** shows the internal wiring of the cable in **Figure 60**. Refer to **Table 24** for the wiring of the connector.

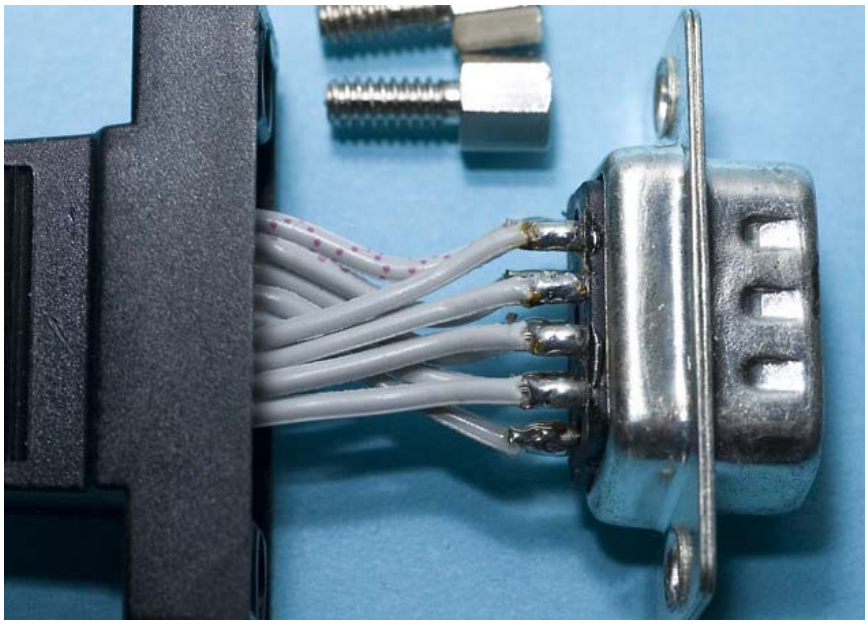

Figure 60. RS232 Cable

Table 24 shows the pinout of the ribbon cable connector.

Table 24. Cable Pinout

Ribbon Cable	DB9
1	1
2	2
3	3
4	4
5	5
6	6
7	7
8	8
9	9
10	10

10.3 USB Hubs

There are no known or anticipated issues with USB hubs. However, it should be noted that a self powered hub is highly recommended. **Table 25** is a list of Hubs that have been tested on the Beagle board.

Table 25. USB Hubs Tested

Supplier	Part Number
IOGEAR	GUH274

10.4 USB Thumb Drives

There are no known or anticipated issues with USB thumb drives. Thumb drives can be plugged directly into the Beagle board. **Table 26** is a list of thumb drives that have been tested on the Beagle board.

Table 26. USB Thumb Drives

Supplier	Part Number

10.5 DVI to HDMI Cables

Figure 61 is a picture of a HDMI to DVI-D cable.

Figure 61. DVI-D to HDMI Cable

Table 27 is the pin numbering of the cable as it relates to the signals used.

Table 27. DVI-D to HDMI Cable

SIGNAL	HDMI	DVI-D

10.6 DVI-D Monitors

There are many monitors that can be used with the Beagle. With the integrated EDID feature, timing data is collected from the monitor to enable the SW to adjust its timings. **Table 28** shows a short list of the monitors that have been tested to date on Beagle. Please check BeagleBoard.org for an up to date listing of the DVI-D monitors as well as information on the availability of drivers.

Table 28. DVI-D Monitors Tested

Manufacturer	Part Number
Dell	

10.7 SD/MMC Cards

Table 29 is a list of SD/MMC cards that have been tested on Beagle. Please check BeagleBoard.org for an up to date listing of the SD/MMC cards that have been tested as well as information on the availability of drivers if required.

Table 29. SD/MMC Cards Tested

Manufacturer	Type	Part Number
Patriot	SD	1GB
Microcenter		

10.8 USB to Ethernet

There are several USB to Ethernet adapters on the market and **Figure 62** shows a few of these devices. These devices can easily add Ethernet connectivity to Beagle by using the USB host interface. These are provided as examples only. Check beagleboard.org for information on devices that have drivers available for them.

Figure 62. USB to Ethernet Adapters

Table 29 provides a list of USB to Ethernet Adapters that could be used with the Beagle. Please check BeagleBoard.org for an up to date listing of the USB to Ethernet devices as well as information on the availability of drivers.

Table 30. USB to Ethernet Adapters

Product	Manufacturer
ASOHOUSB	Airlink
TU-ET100C 10/100Mbps	TRENDnet
SABRENT	NB-USB20

10.9 USB to WiFi

There are several USB to WiFi adapters on the market and **Figure 63** shows a few of these devices. These devices can easily add WiFi connectivity to Beagle by using the USB host interface. These are provided as examples only. Check beagleboard.org for information on devices that have drivers available for them.

Figure 63. USB to WiFi

Table 30 provides a list of USB to WiFi adapters that could be used with the Beagle. Please check BeagleBoard.org for an up to date listing of the USB to Wifi devices as well as information on the availability of drivers.

Table 31. USB to WiFI Adapters

Product	Manufacturer
4410-00-00AF	Zoom
HWUG1	Hawkins
TEW-429Uf	Trendnet

10.10 USB to Bluetooth

There are several USB to Bluetooth adapters on the market and **Figure 64** shows a few of these devices. These devices can easily add Bluetooth connectivity to Beagle by using the USB host interface. These are provided as examples only. Check beagleboard.org for information on devices that have drivers available for them and their test status.

Figure 64. USB to Bluetooth

Table 30 provides a list of USB to Bluetooth adapters that could be used with the Beagle. Please check BeagleBoard.org for an up to date listing of the USB to Bluetooth devices as well as information on the availability of drivers.

Table 32. USB to Bluetooth Adapters

Product	Manufacturer
TBW-105UB	Trendnet
ABT-200	Airlink
F8T012-1	Belkin

10.11 USB to Card Reader

There are several USB Card Reader adapters on the market and **Table 33** shows a few of these devices that have been tested to date. Check beagleboard.org for information on devices that have drivers available for them and their test status.

Table 33. USB Card Readers

Manufacturer	Product
idotConnect	Card Reader/Writer (Multi)

10.12 Expansion Cards

This section is provided for future use as expansion cards are released for the Beagle.

11.0 Mechanical Information

11.1 Beagle Dimensions

This section provides information on the mechanical aspect of the Beagle. Dimensions for the Beagle are provided here. **Figure 65** is the dimensions of the Beagle.

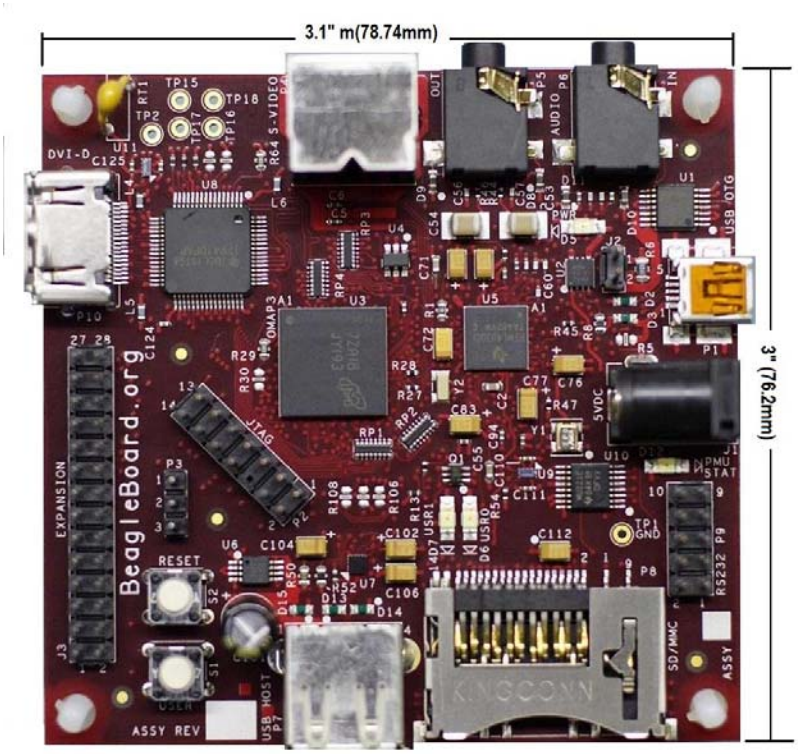

Figure 65. Beagle Dimension Drawing

11.2 Beagle Daughter Card Information

This section provides information on what is required from a mechanical aspect to create a daughter card for the Beagle. Users are free to create their own cards for private or commercial use. The concept of a standard card size for these cards is not being set down. The examples provided in this section show what is possible and is provided as a starting point. The idea is not to limit the possibilities.

11.2.1 Stacked Daughtercard Card

One method is to provide a daughtercard stacked onto the board. This can be either mounted on top of the Beagle or under the Beagle. **Figure 66** and **Figure 6**7 shows these two strategies.

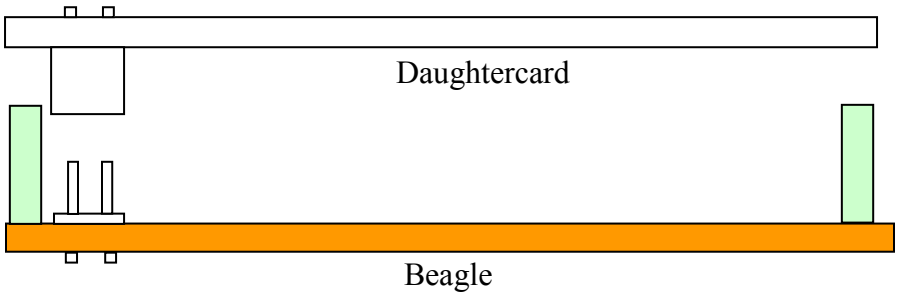

Figure 66. Beagle Top Stacked Daughter Card

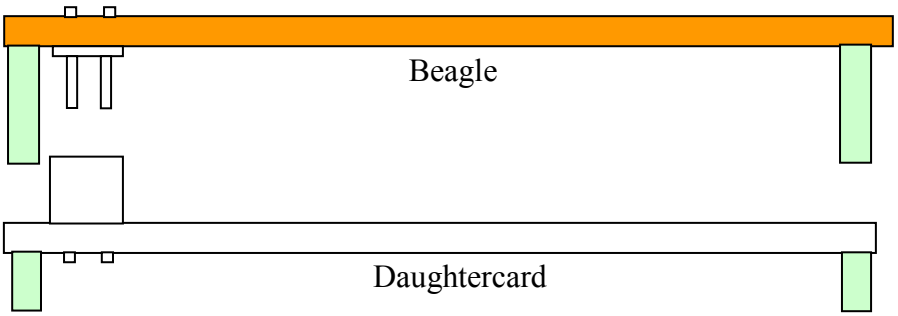

Figure 67. Beagle Bottom Stacked Daughter Card

11.2.2 Offset Daughter Card Information

Another option is to create a daughtercard that plugs in from the side. **Figure 68** and **Figure 69** shows the offset daughtercard using a board to board connector system.

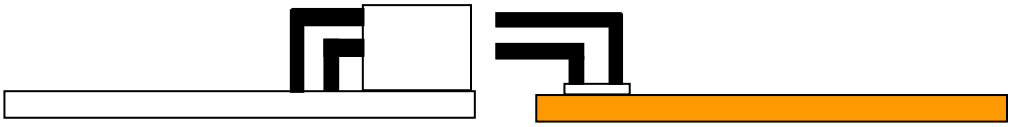

Figure 68. Beagle Offset Daughter Card Side

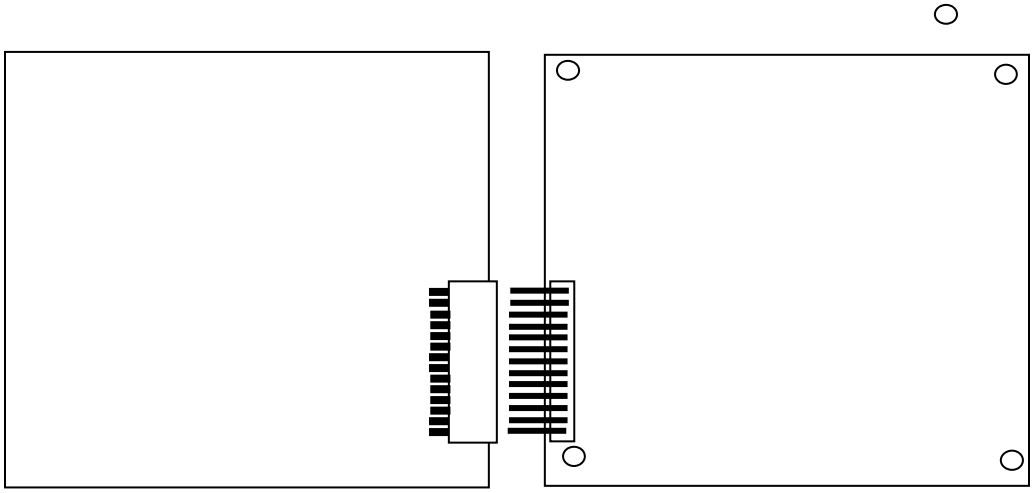

Figure 69. Beagle Offset Daughter Card Top

11.2.3 Ribbon Cable Daughter Card Information

Another method is to use a ribbon cable to connect the two boards together. **Figure 70** shows this concept.

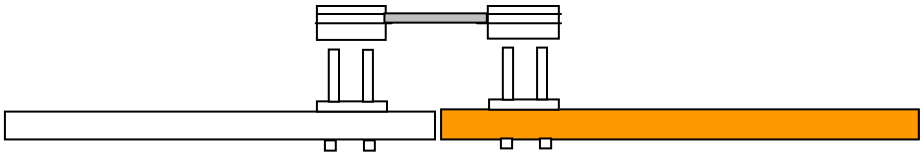

Figure 70. Ribbon Cable Daughter Card

12.0 Troubleshooting

This section will provide assistance in troubleshooting the Beagle in the event there are questions raised as to what the sate of the Beagle is. This may be due to a HW failure or the SW not initializing things properly during development. Also provided is a section of know issues. Be sure and check with beagleboard.org for any updates.

12.1 Access Points

This section covers the various access points where various signals and voltages can be measured.

12.1.1 Voltage Points

Figure 71 shows the test points for the various voltages on Beagle.

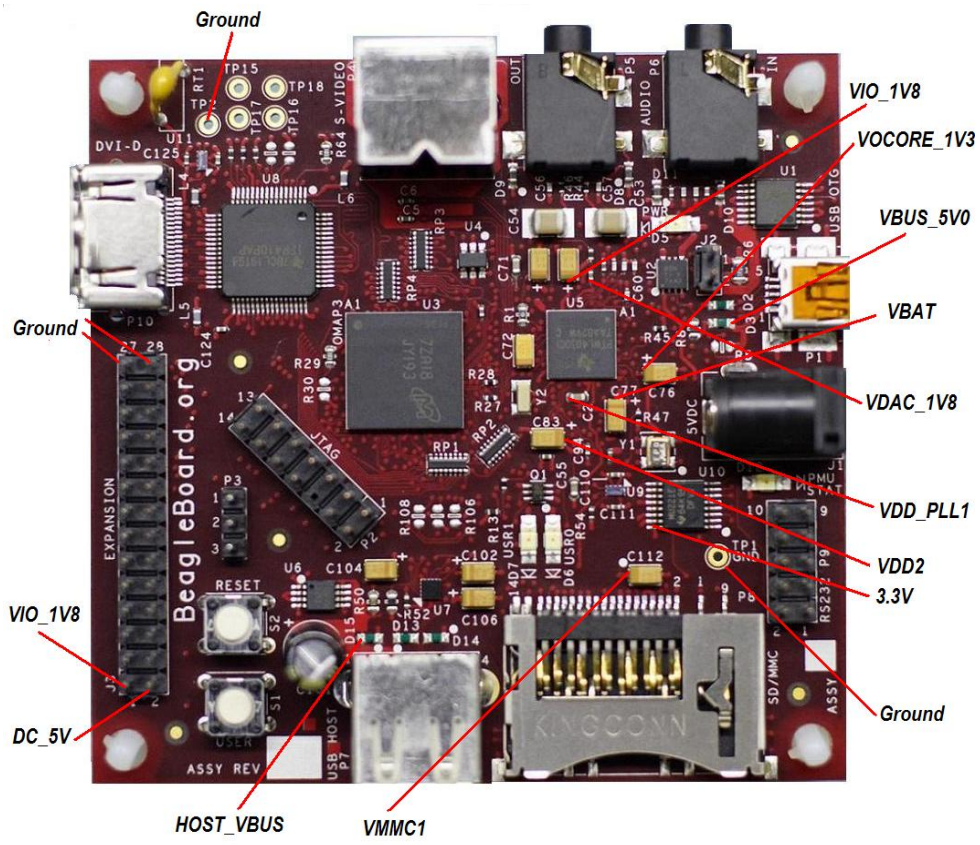

Figure 71. Beagle Voltage Access Points

Some of these voltages may not be present depending on the state of the TWL4030 as set by the OMAP3. Others may be at different voltage levels depending on the same factor.

Table 33 provides the ranges of the voltages and the definition of the conditions as applicable.

Table 34. Voltages

Voltage	Min	Nom	Max	Conditions
VIO_1V8	1.78	1.8	1.81	
VDD_SIM	1.78	1.8	1.81	
VBUS_5V0	4.9	5.0	5.5	From the host PC. May be lower or higher.
VOCORE_1V3	1.15	1.2	1.25	Can be set via SW. Voltage levels may vary.
VBAT	4.1	4.2	4.3	
VDAC_1V8	1.78	1.8	1.81	
VDD_PLL1	1.78	1.8	1.81	
VDD_PLL2	1.78	1.8	1.81	
VDD2	1.15	1.2	1.25	
3.3V	3.28	3.3	3.32	
VMMC1 (3V)	2.9	3.0	3.1	3.0V at power up. Can be set to via SW.
VMMC1(1.8V)	1.78	1.8	1.81	
HOST_VBUS	4.9	5.0	5.5	Must be activated via SW. Will be based on either the USB voltage from the PC or the DC supply voltage levels.

12.1.2 Signal Access Points

Figure 72 shows the access points for various signals on Beagle.

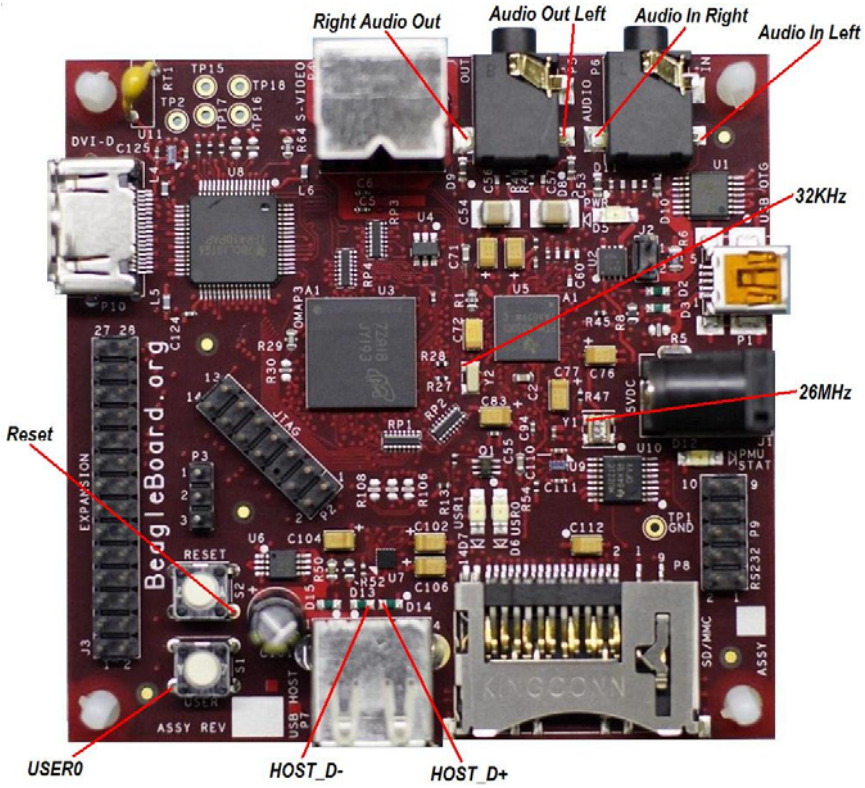

Figure 72. Beagle Signal Access Points

12.2 Troubleshooting Guide

Table 35 provides a list of possible failure modes and conditions and suggestions on how to diagnose them and ultimate determine whether the HW is operational or not.

Table 35. Troubleshooting

Symptoms	Possible Problem	Action
JTAG does not connect.	Verify that the Power LED is on.	If off and running over USB, the PC may have shut down the voltage due to excessive current as related to what it is capable of providing. Remove the USB cable and re insert. If running on a DC supply make sure that voltage is being supplied.
	JTAG interface needs to be reset	Reset the Beagle.
UBoot does not start, and no activity on the RS232 monitor.	Incorrect serial cable configuration.	Verify orientation of the RS232 flat cable
		Check for the right Serial twist cable.
	If a 40T is displayed over the serial cable, processor is booting. Issue could be the SD/MMC card.	Make sure the SD/MMC card is installed all they way into the connector.
USB Host Connection Issues	Cheap USB Cable. OTG cables are typically not designed for higher current. The expect 100mA max.	Measure the voltage at the card to determine the voltage drop across the cable. If it the level is below 4.35V, the USB is not guaranteed to work,

13.0 Known Issues

This section provides information on any know issues with the Beagle HW and the overall status. **Table 36** provides a list of the know issues on the Beagle.

Table 36. Known Issues

Affected Revision	Issue	Description	Workaround	Final Fix
A5	DC Connector does not work.	There is a layout issue where the pins were swapped on the schematic symbol.	Use USB power only.	Rev B
A5	USER0 and USER1 LEDs are shorted.	USER0 and USER1 cannot be controlled separately due to an issue in the PCB causing them to be shorted.	None	Rev B

14.0 PCB Component Locations

Figures 73 and **Figure 74** contain the bottom and top side component locations of the Beagle.

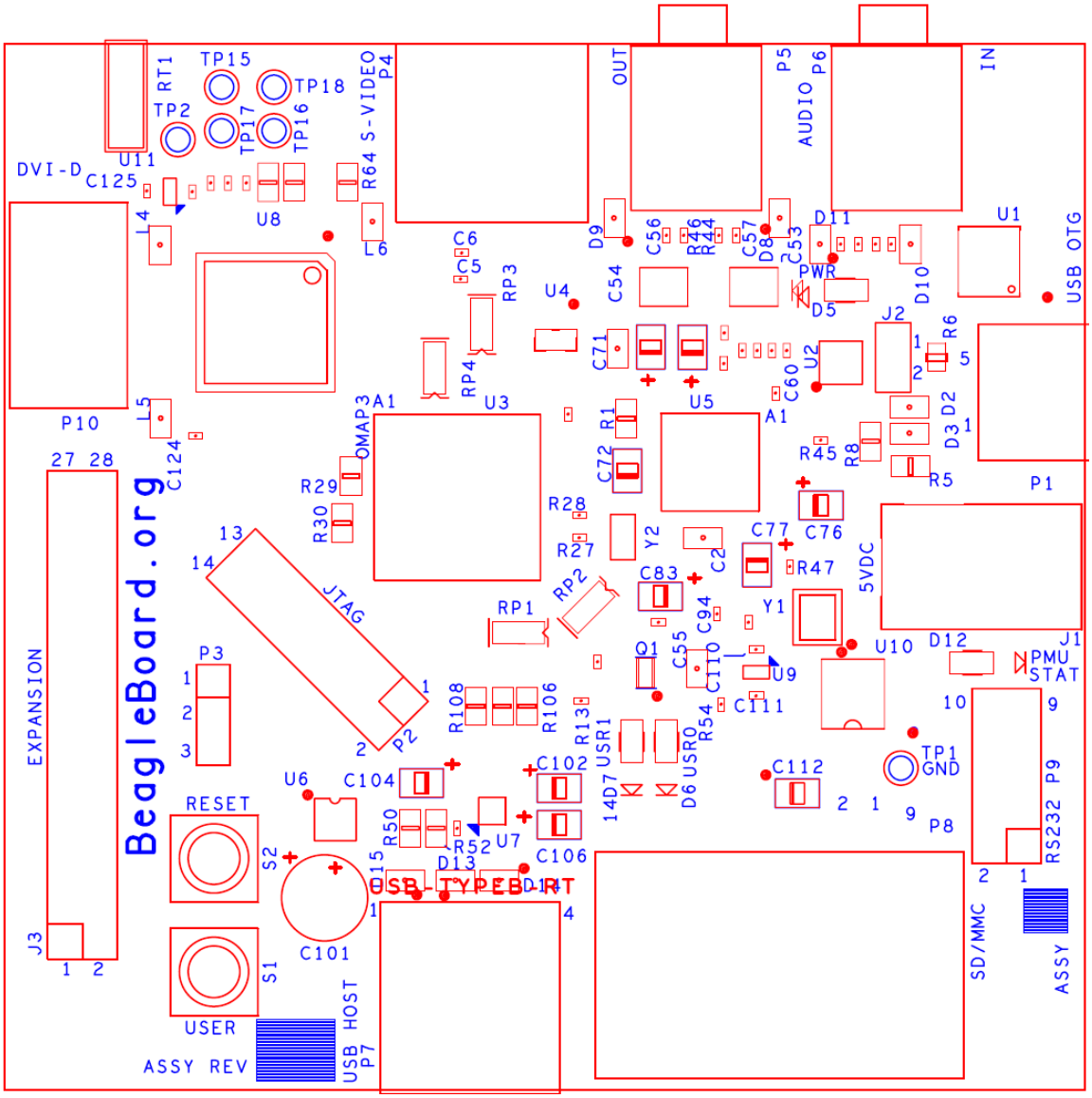

Figure 73. Beagle Top Side Components

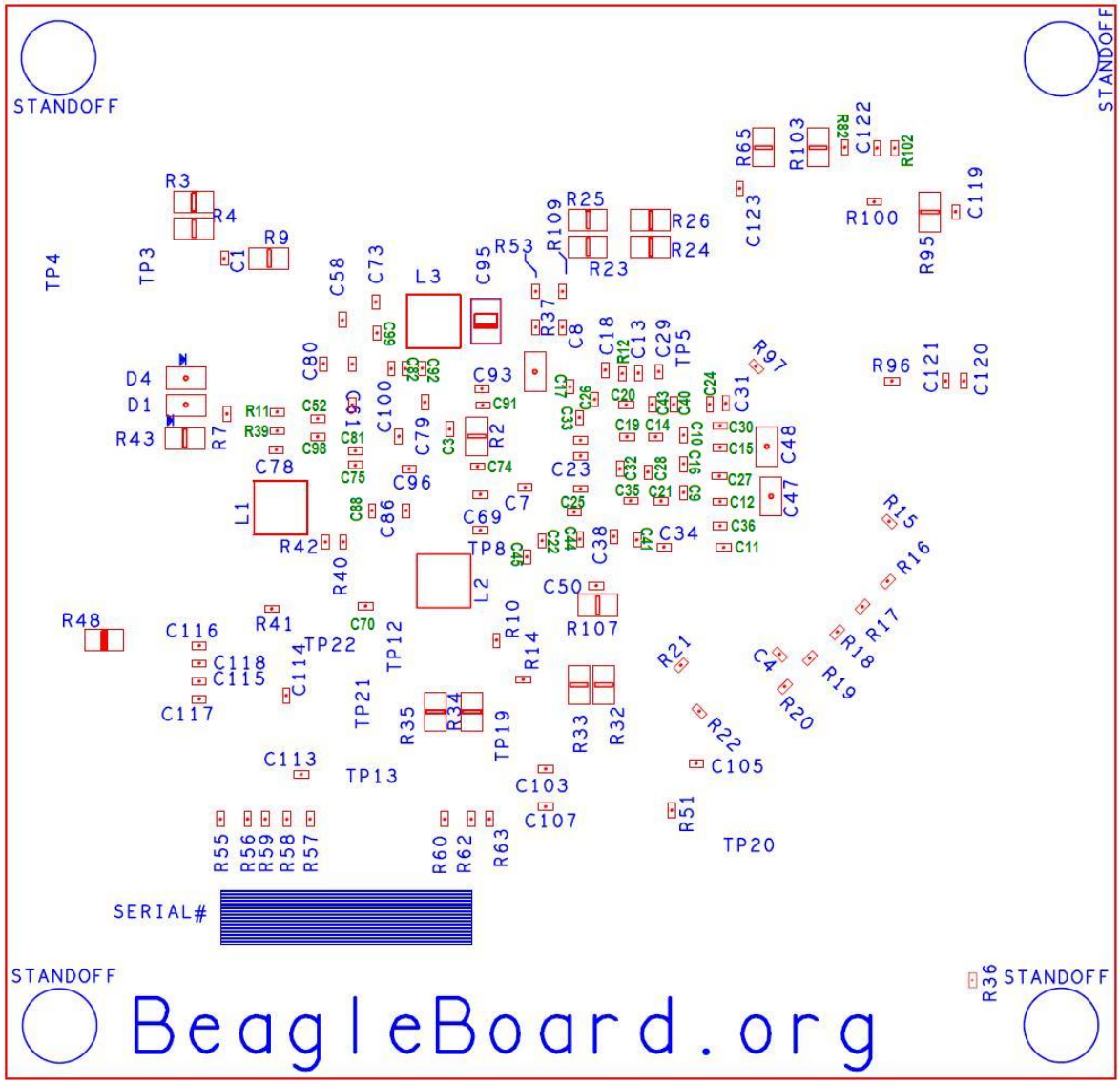

Figure 74. Beagle Bottom Side Components

The reference designators in green are not on the PCB. These were added to the figure.

15.0 Schematics

The following pages contain the PDF schematics for the Beagle. This manual will be periodically updated, but for the latest documentations be sure and check beagleboard.org for the latest schematics.

OrCAD source files will be provided for Beagle on beagleboard.org.

REV	DESCRIPTION	DATE	BY
A	Formal Release of the schematic.	2/1/08	GC
A1	Resistor values on all LEDS were normalized to 200 ohms to keep brightness levels the same.	2/15/08	GC
A2	Resistor loading for the S-Video output was set for ES2.0 silicon. Changed resistor loading to match ES2.1 silicon used. Made R24 and R25 as DNI. Made R23 and R26 as installed.	2/23/08	GC
A3	Changed R11,R12, R13, and R14 to 4.7K to boost drive on I2C. Changed R53 to DNI as it is not needed.	3/2/08	GC
A4	Changed C101 from 100uF to 47uF to lower the volatge drain when turned on by SW.	3/24/08	GC
A5	Incorrect part installed in L1 and L3. Replaced those parts on the boards. Changed R6 for a 1.0 ohm to a .1 ohm t reduce volatge drop at higher currents.	4/7/08	GC

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2	USB OTG CONNECTOR AND MAIN POWER
3	OMAP3 1 OF 3
4	OMAP3 2 OF 3, JTAG, SWITCHES, LEDS, SVIDEO
5	OMAP3 3 OF 3
6	TWL4030 1 of 2, AUDIO JACKS, LED, 26MHZ, 32KHZ
7	TWL4030 2 of 2
8	USB HOST, EXPANSION
9	SD/MMC, SERIAL HEADER
10	DVI-D

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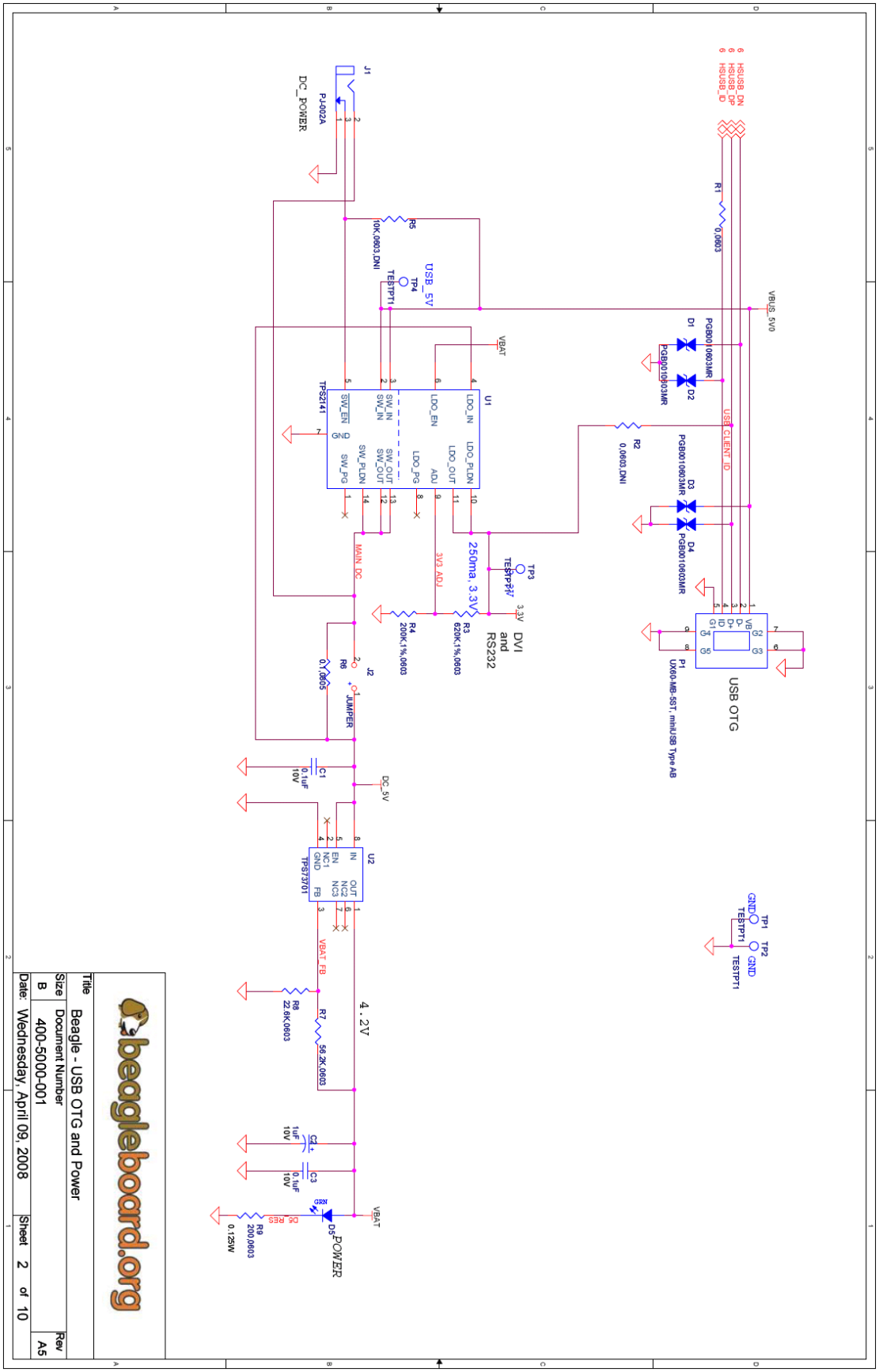
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Beagle - USB OTG and Power
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DC_POWER
USB_5V
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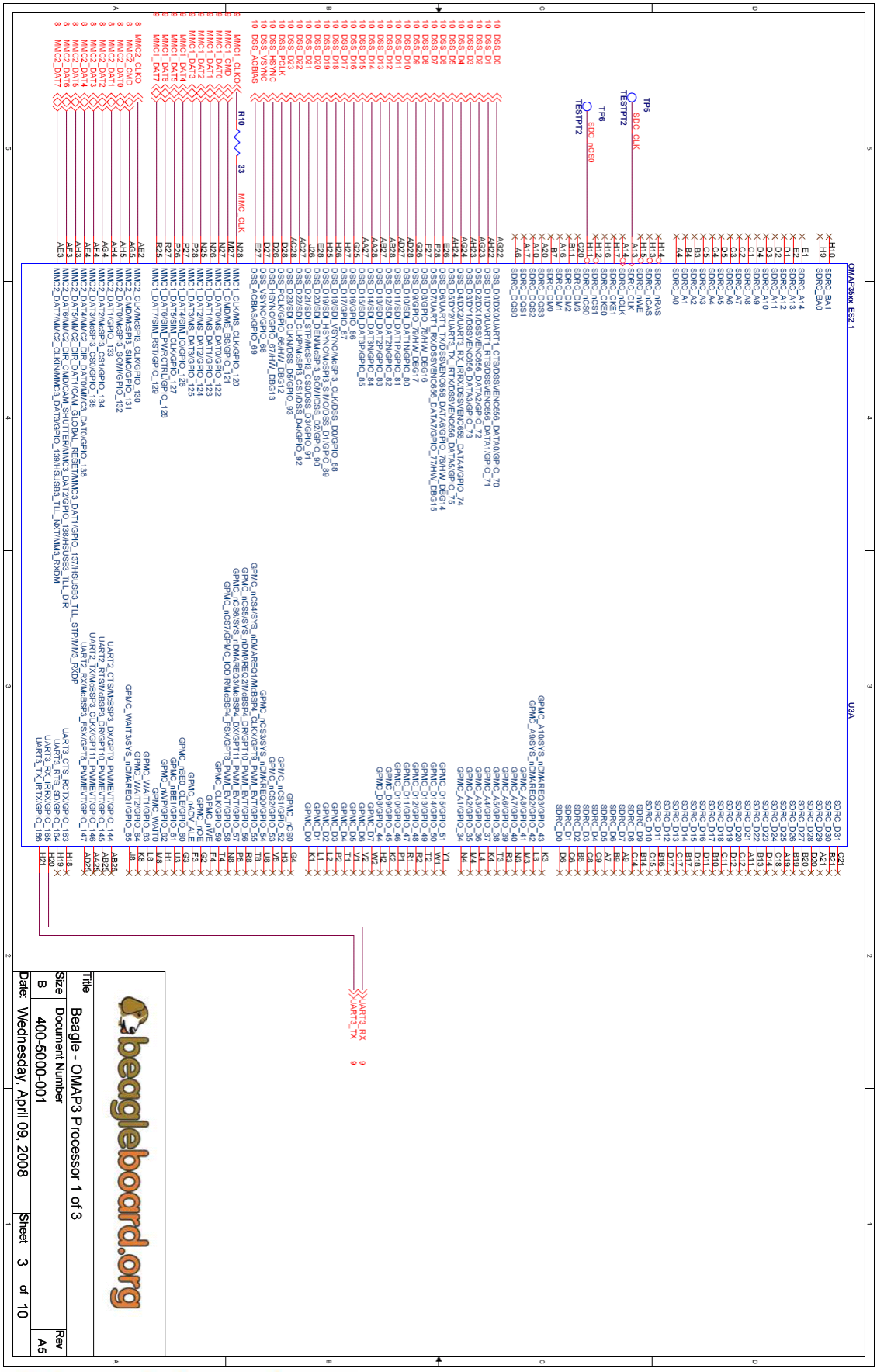
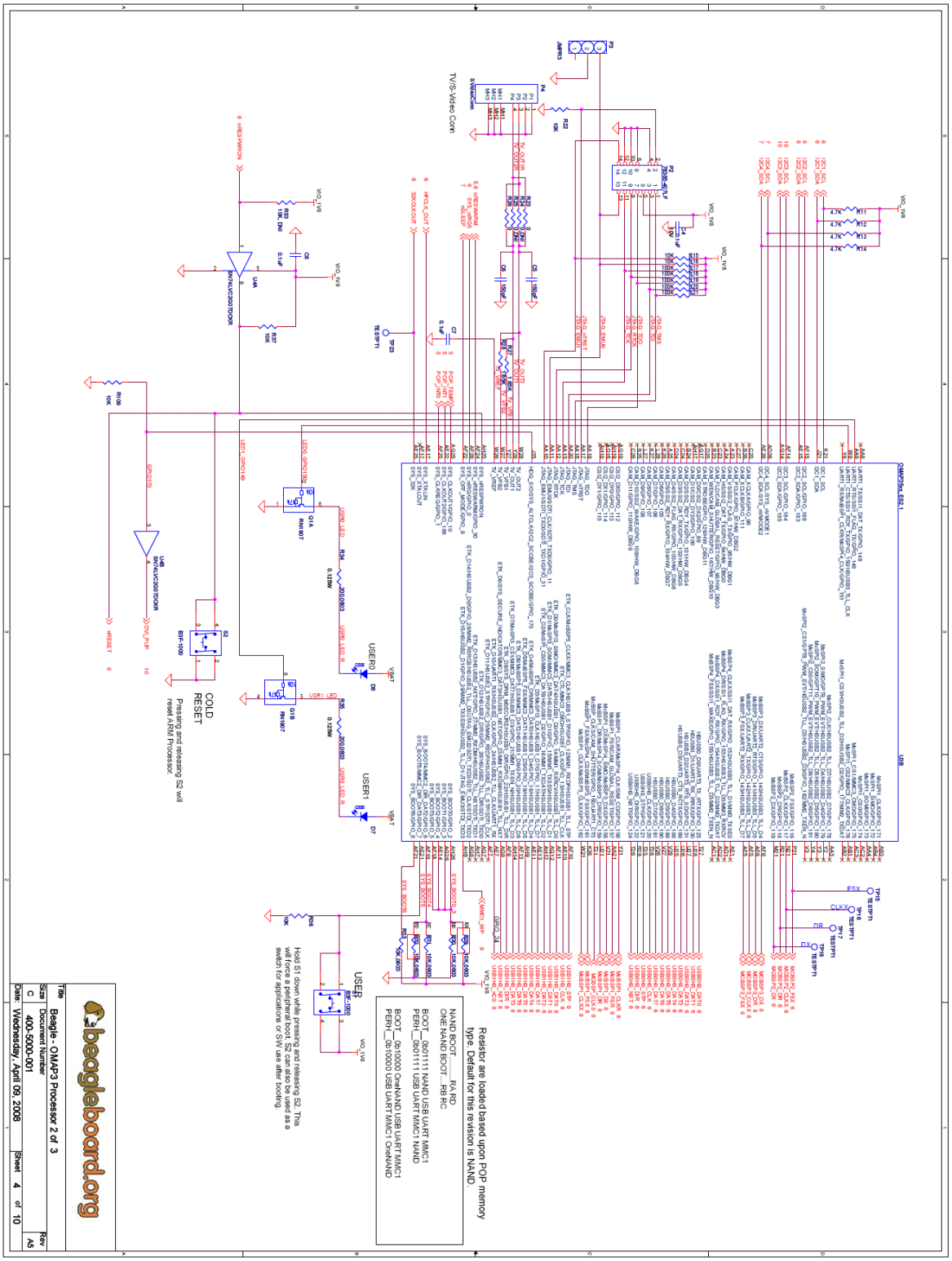
JUMPER
TPS2141
TPS73701


OMAP35x ES2.1
U3A
beagleboard.org
Beagle - OMAP3 Processor 1 of 3
Document Number
400-5000-001
Rev
A5
Size
B
Date: Wednesday, April 09, 2008
Sheet 3 of 10


beagleboard.org
Title
Beagle - OMAP3 Processor 2 of 3
Size
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Document Number
400-5000-001
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A5
Date: Wednesday, April 09, 2008
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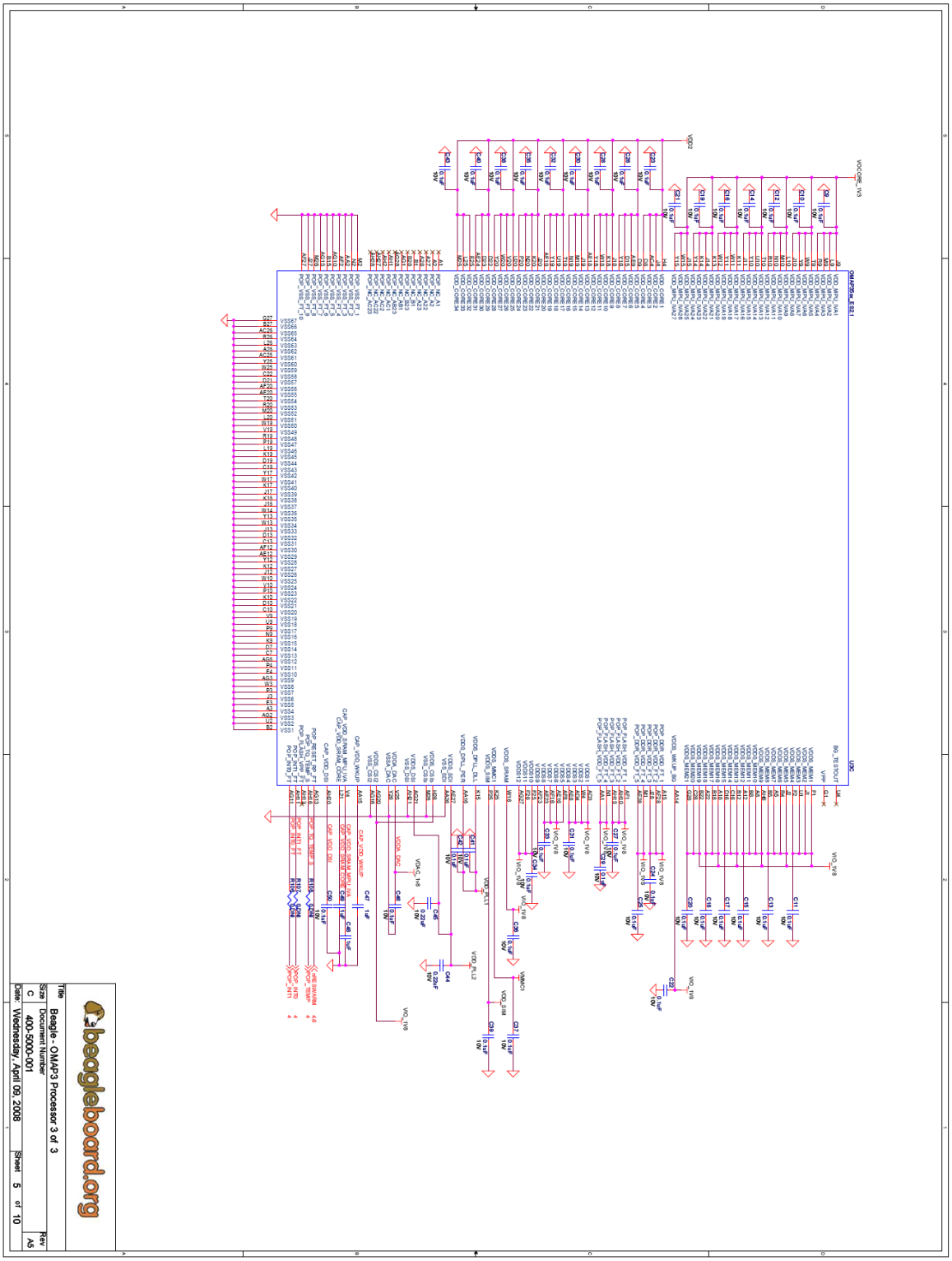
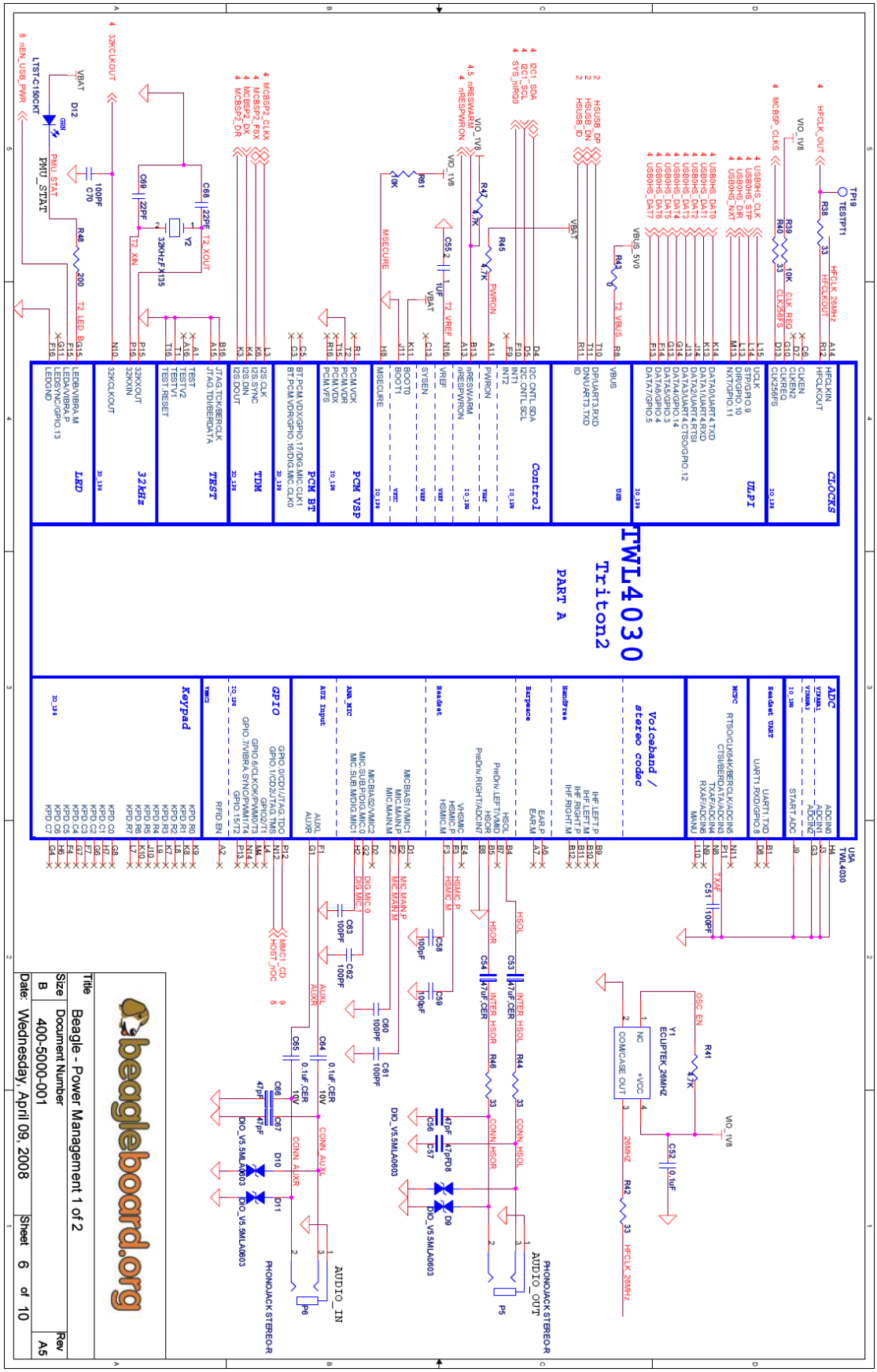
TV/S-Video Conn
COLD RESET
Pressing and releasing S2 will reset ARM Processor.
USER0
USER1
USER
Hold S1 down while pressing and releasing S2. This will force a peripheral boot. S2 can also be used as a switch for applications or SW use after booting.
Resistor are loaded based upon POP memory type. Default for this revision is NAND.
NAND BOOT.....RA RD
ONE NAND BOOT....RB RC
BOOT_0b01111 NAND USB UART MMC1
PERH_0b01111 USB UART MMC1 NAND
BOOT_0b10000 OneNAND USB UART MMC1
PERH_0b10000 USB UART MMC1 OneNAND


beagleboard.org
Title
Beagle - OMAP3 Processor 3 of 3
Size
C
Document Number
400-5000-001
Rev
A5
Date: Wednesday, April 09, 2008
Sheet 5 of 10


TWL4030
Triton2
PART A
Control
CLOCKS
USB ULPI
ADC
Audio UART
MCSPI
Voiceband / stereo codec
Earpiece
Headset
Handfree
AUX Input
GPIO
Keypad
PCM VSP
PCM BT
TDM
32KHz
TEST
LED
Beagle - Power Management 1 of 2
Document Number
400-5000-001
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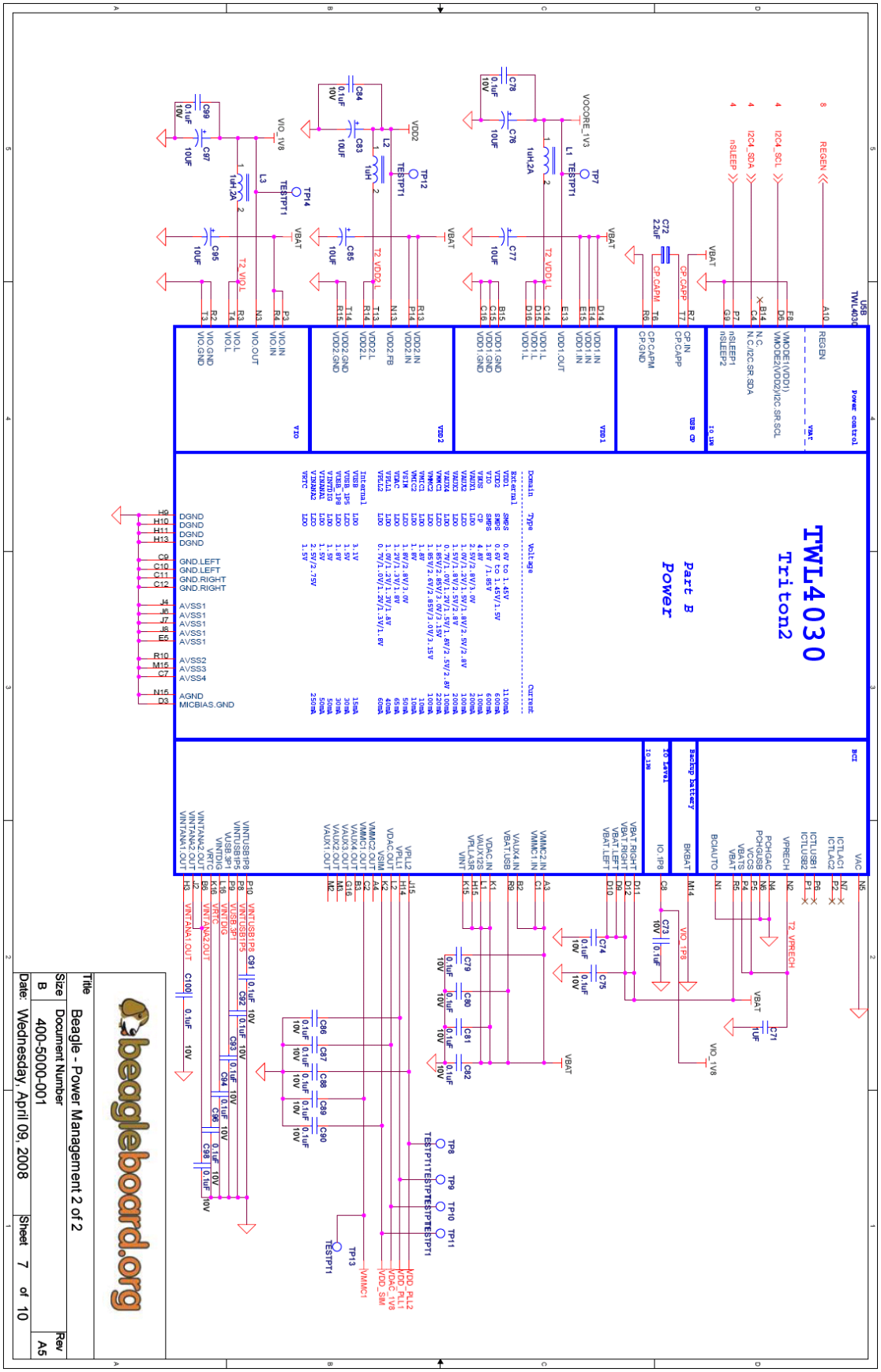
Date: Wednesday, April 09, 2008
Sheet 6 of 10
beagleboard.org


TWL4030
Triton2
Part B
Power
Power control
Backup battery
IO Level
BCI
Title
Beagle - Power Management 2 of 2
Size
B
Document Number
400-5000-001
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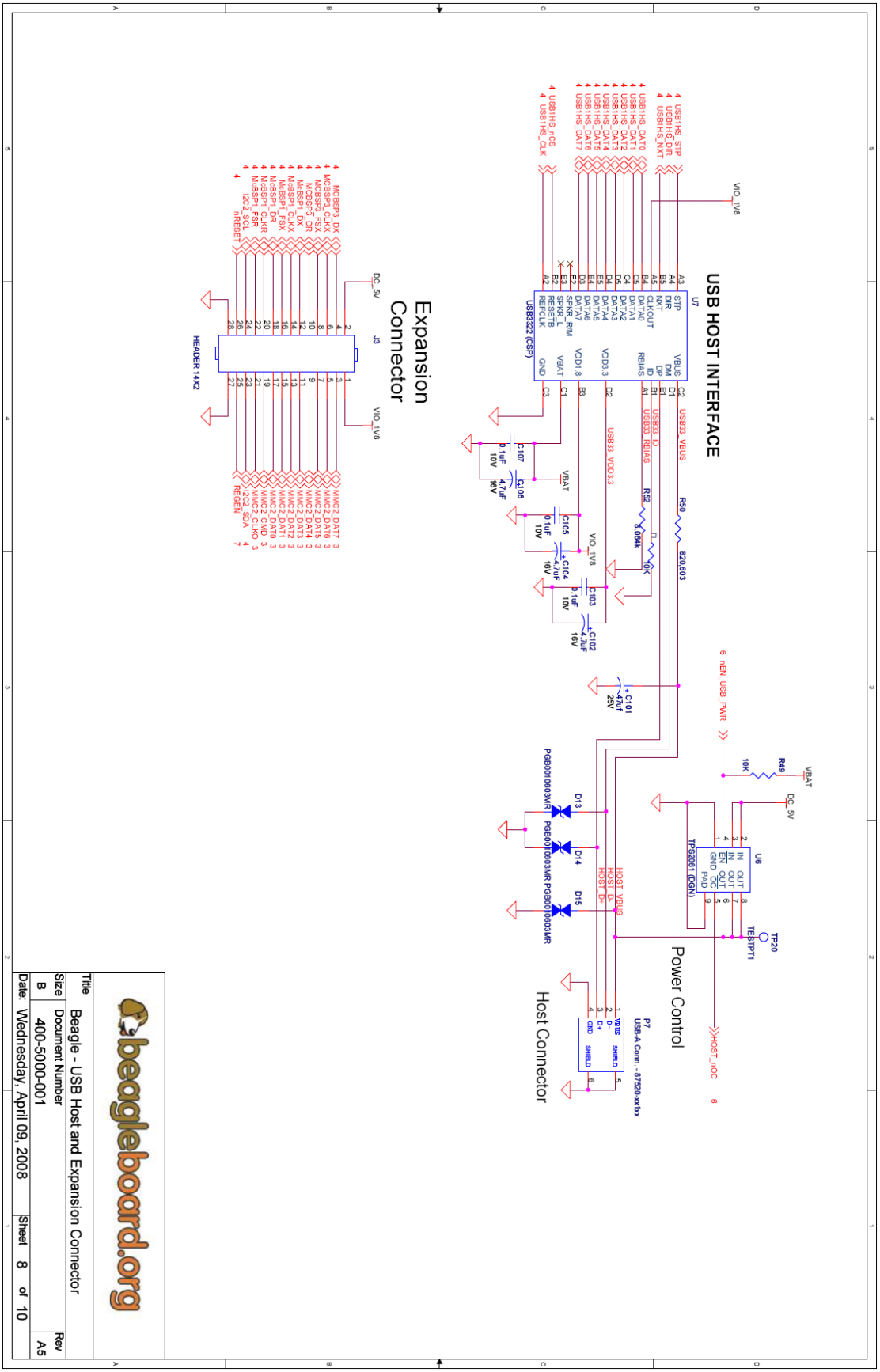
beagleboard.org


USB HOST INTERFACE
Expansion Connector
Power Control
Host Connector
beagleboard.org
Title
Beagle - USB Host and Expansion Connector
Size
B
Document Number
400-5000-001
Rev
A5
Date: Wednesday, April 09, 2008
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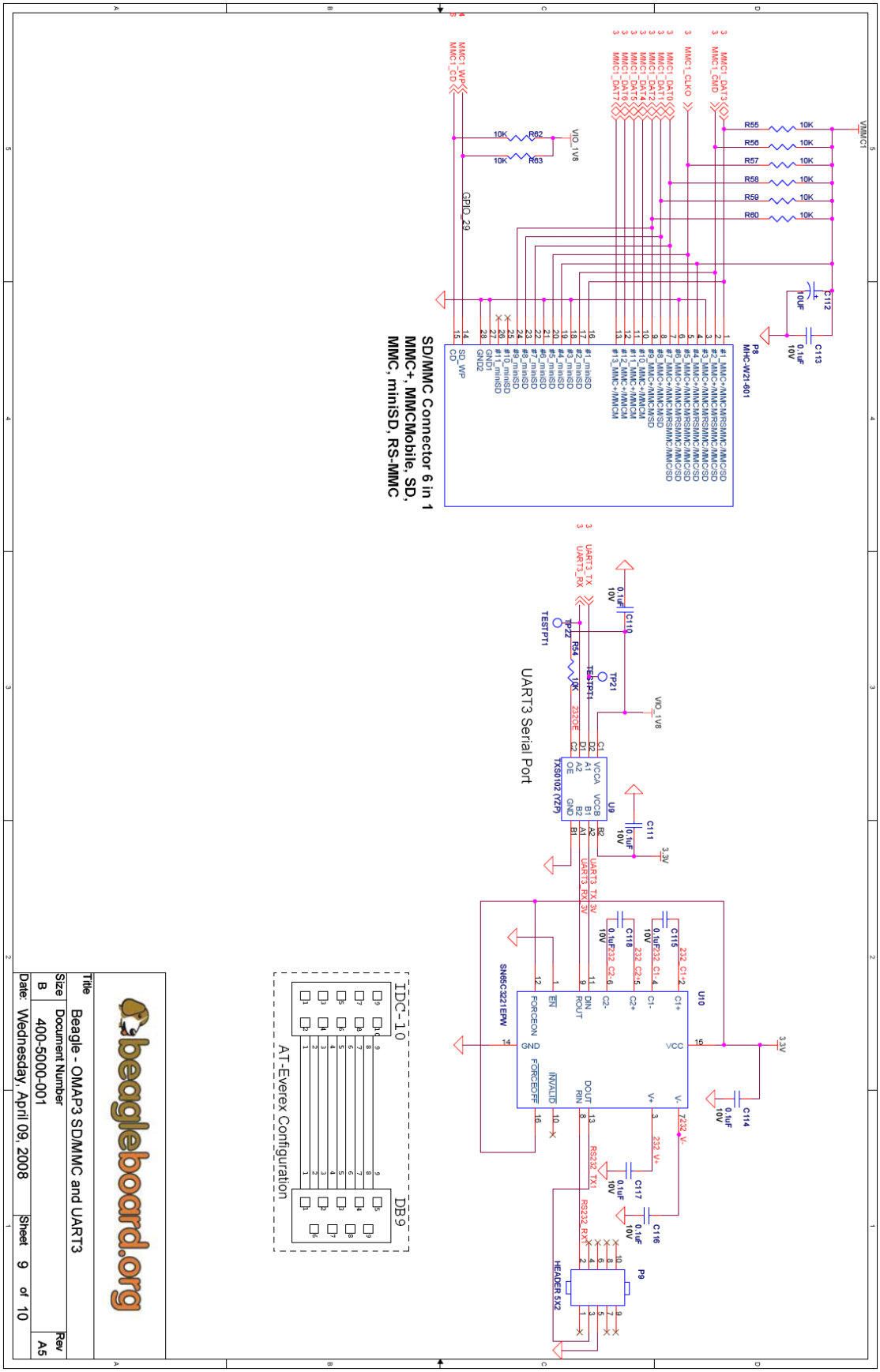
SD/MMC Connector 6 in 1
MMC+, MMCMobile, SD,
MMC, miniSD, RS-MMC
UART3 Serial Port
AT-Everex Configuration
IDC-10
DB9
beagleboard.org
Beagle - OMAP3 SD/MMC and UART3
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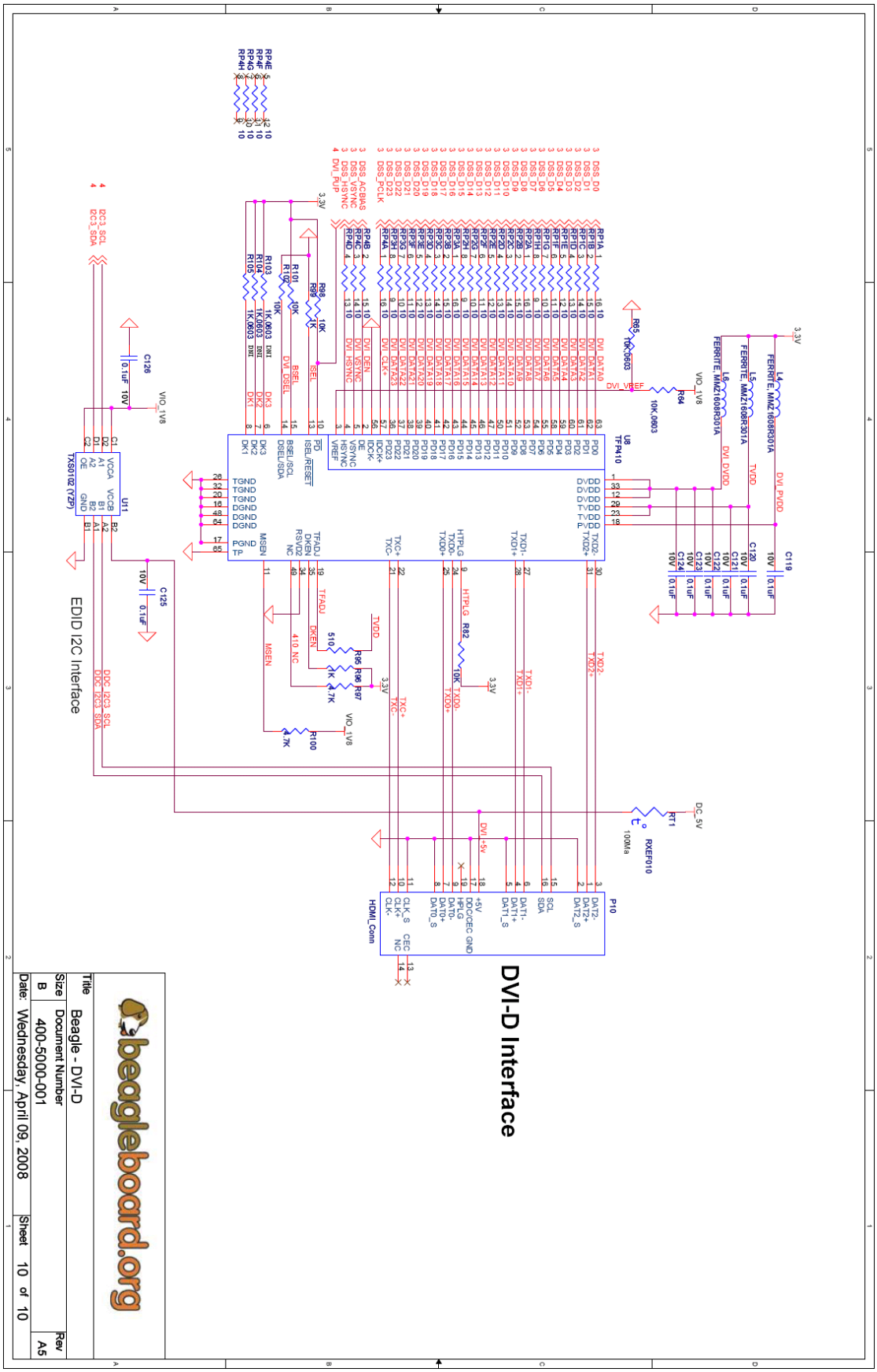
DVI-D Interface
EDID I2C Interface
beagleboard.org
Beagle - DVI-D
Document Number
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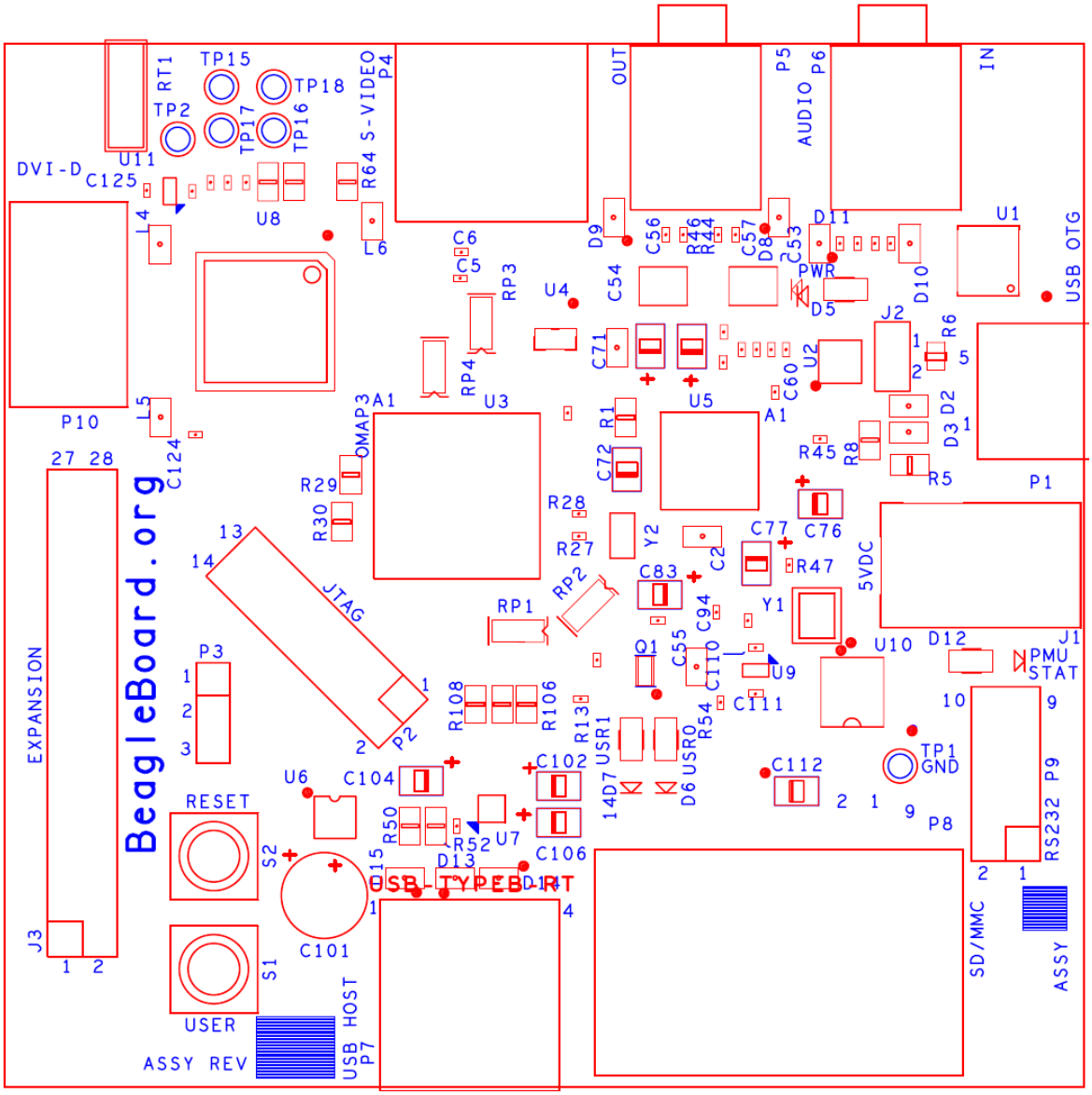
Date: Wednesday, April 09, 2008
Sheet 10 of 10

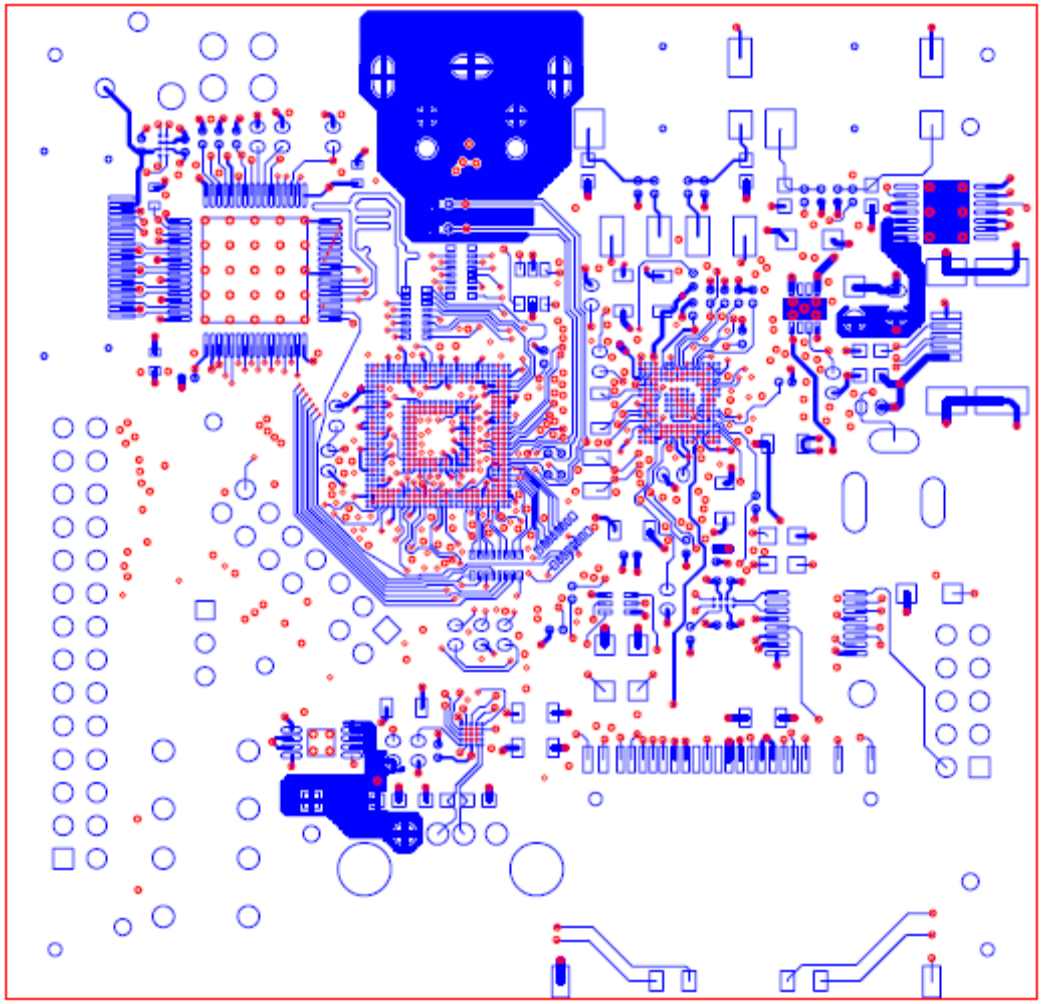
16.0 PCB Information

The following pages contain the PDF PCB layers for the Beagle. Gerber files and Allegro source files are available on beagleboard.org.

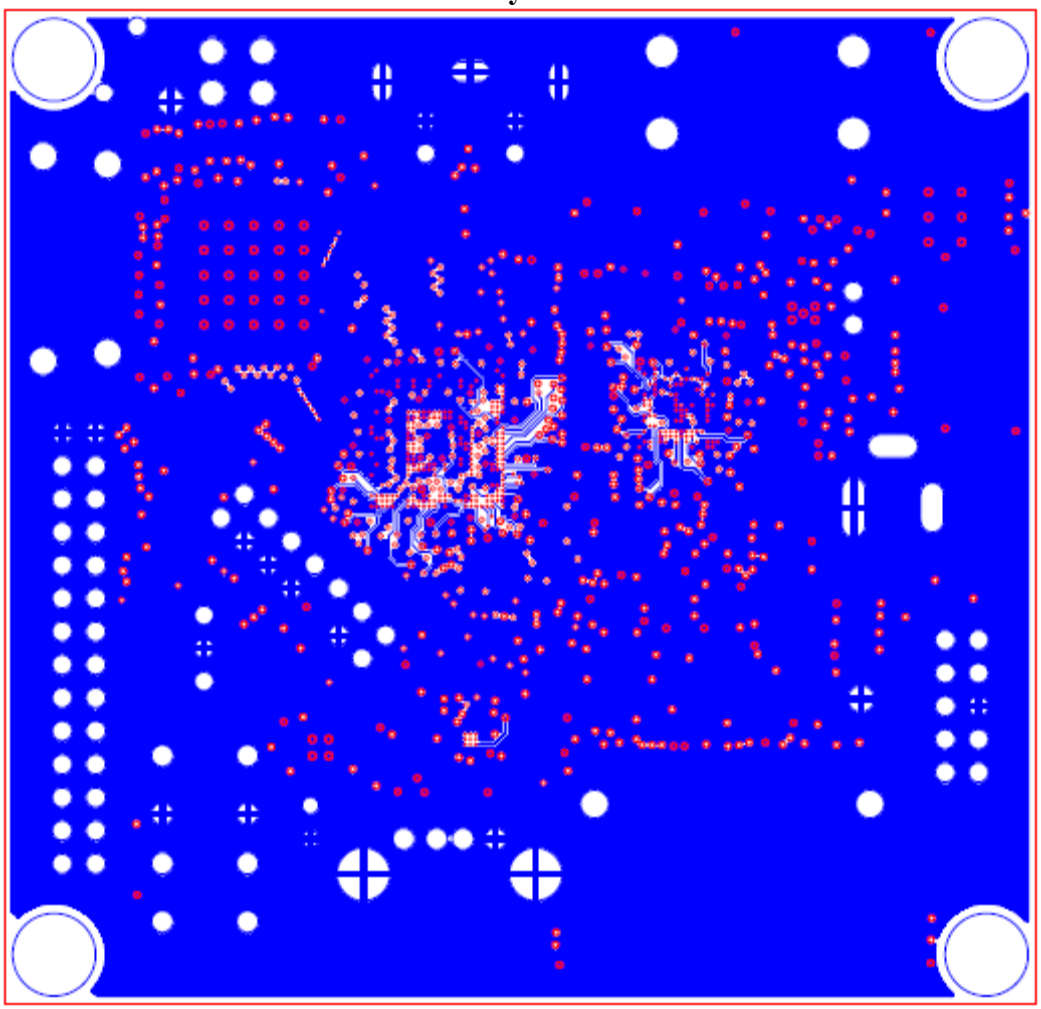
Top Silkscreen



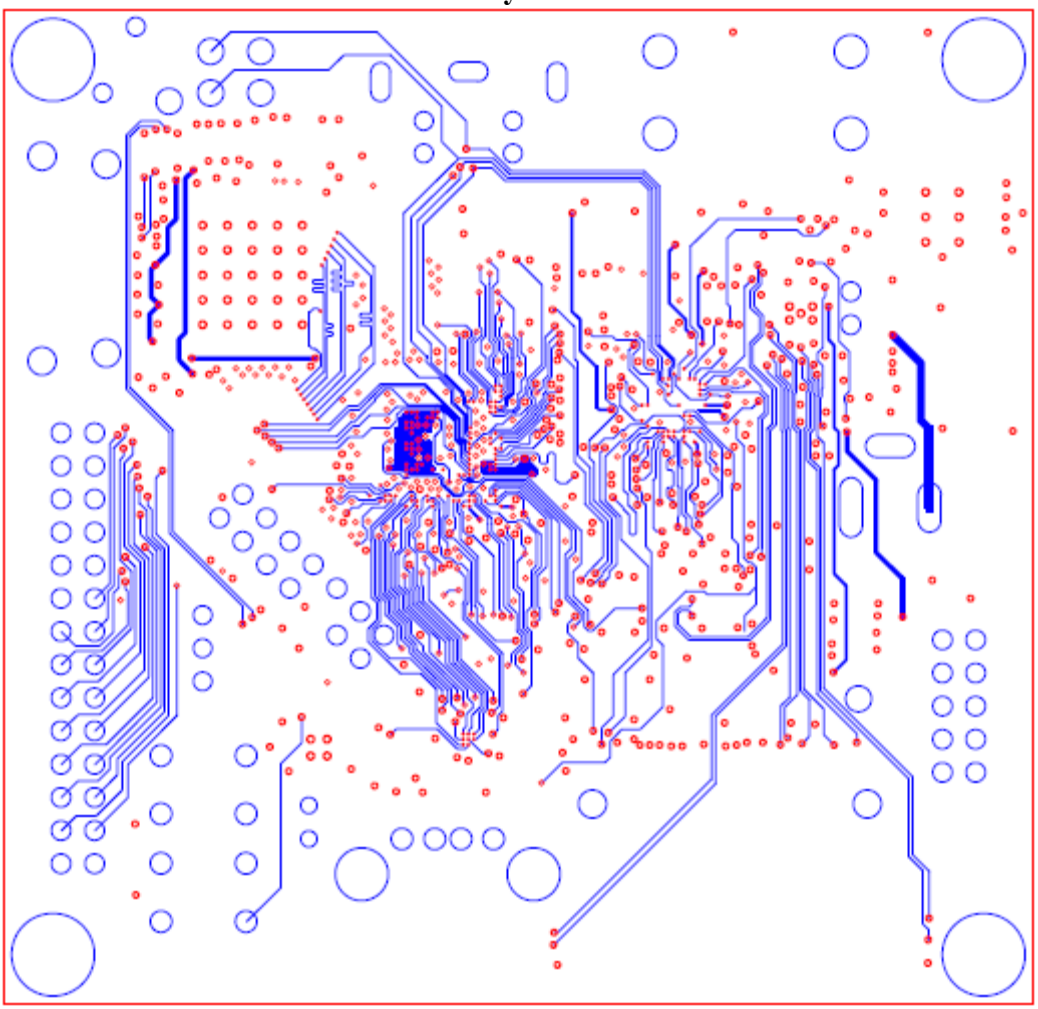
Layer 1



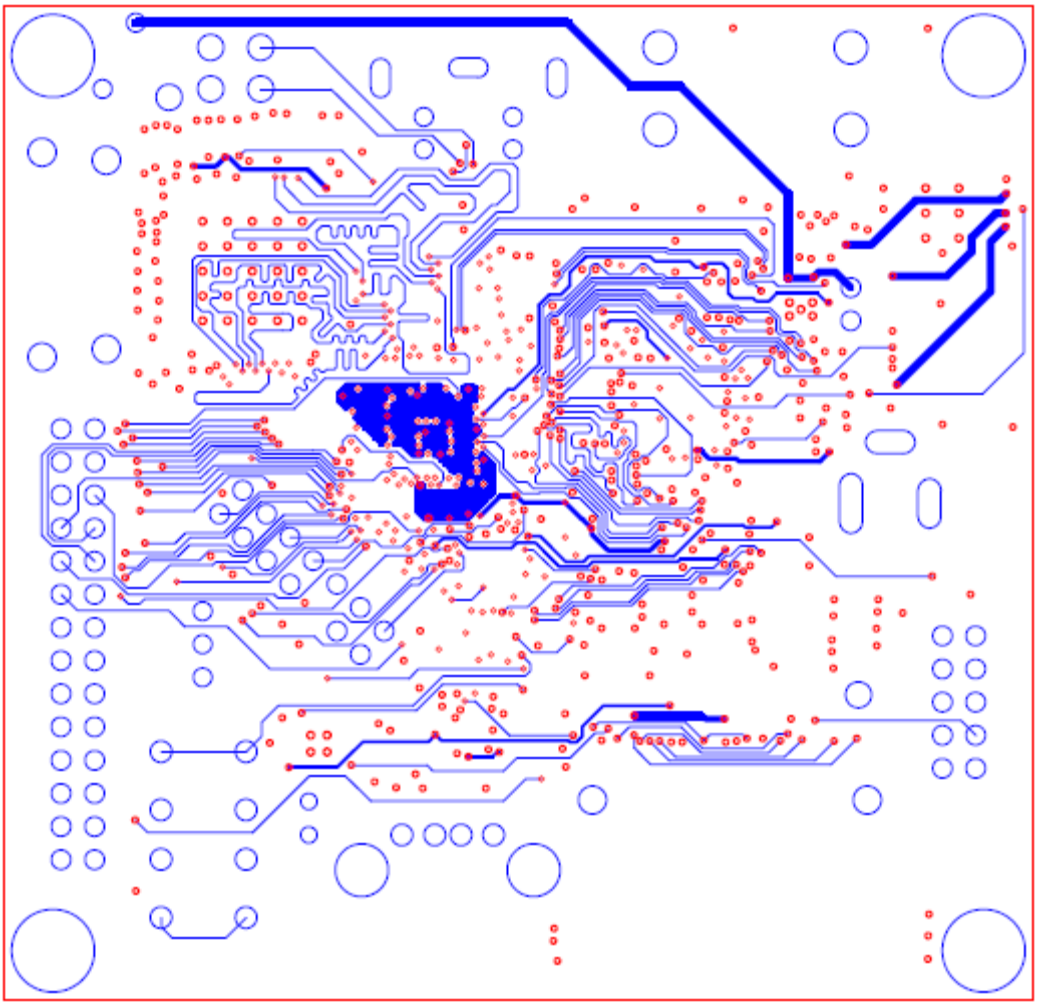
Layer 2



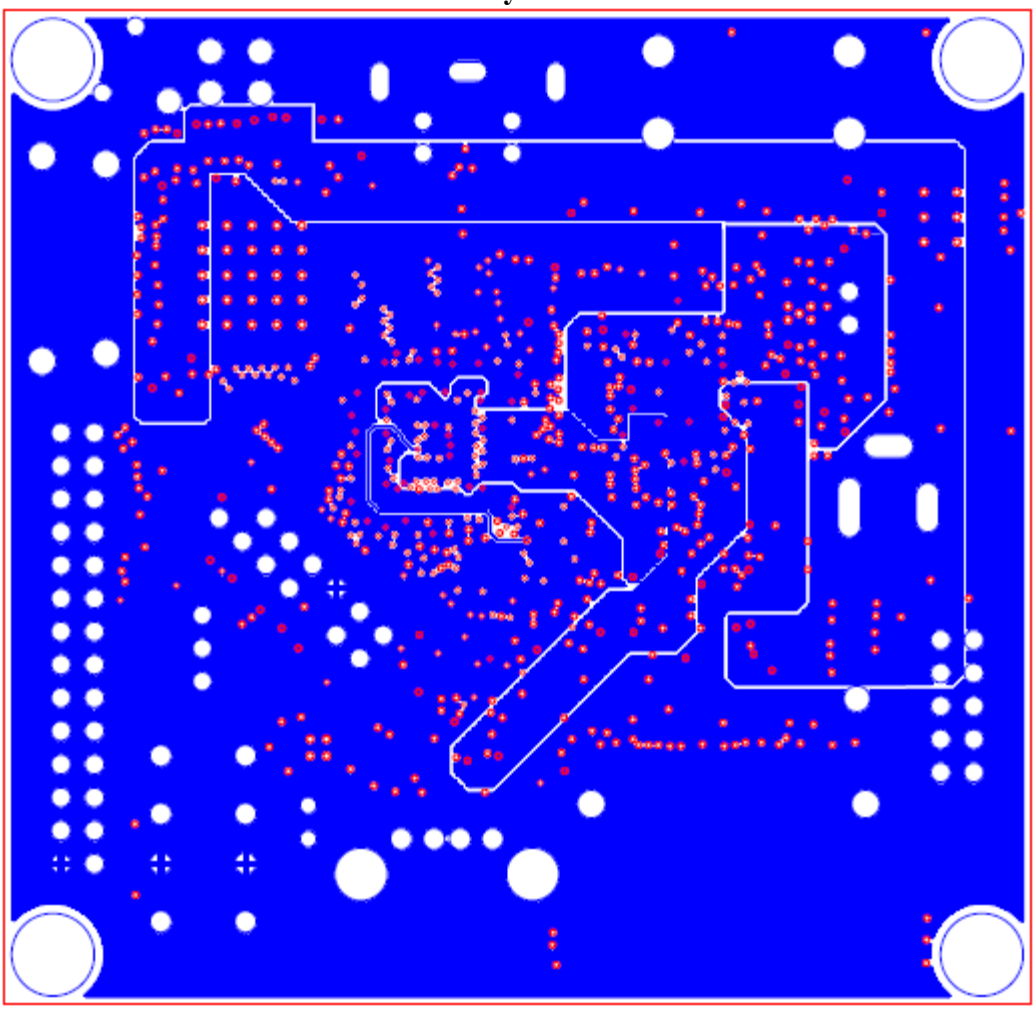
Layer 3



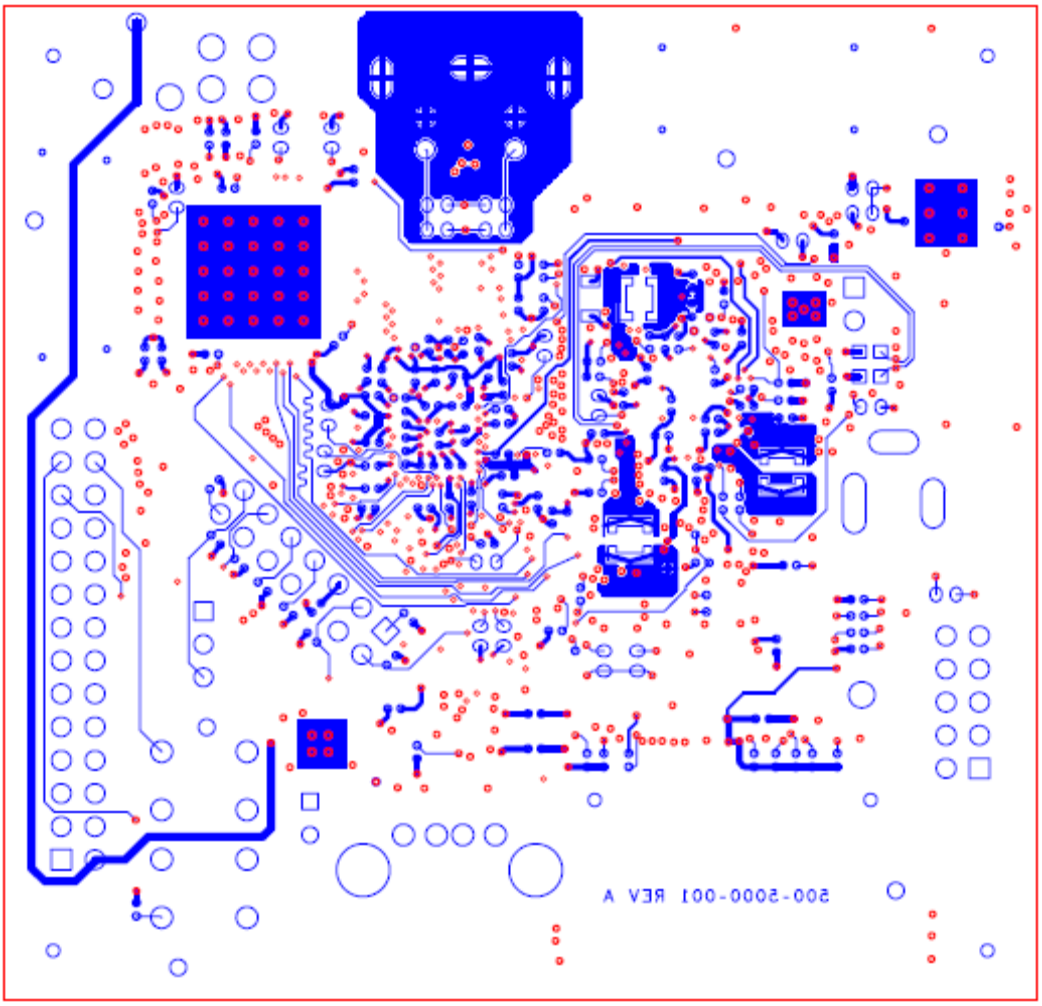
Layer 4



Layer 5



Layer 6



Bottom Silkscreen